

UTILITY
PATENT APPLICATION
TRANSMITTAL

Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 35.C12475 Div. I

First Named Inventor or Application Identifier

KATSUMI NAKAGAWA ET AL.

Express Mail Label No.

APPLICATION ELEMENTS

MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO:

Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☐ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. ☒ Specification Total Pages 112

3. ☒ Drawing(s) (35 USC 113) Total Sheets 10

4. ☒ Oath or Declaration Total Pages 2

a. ☐ Newly executed (original or copy)

b. ☐ Unexecuted for information purposes

c. ☒ Copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 17 completed)
[Note Box 5 below]

i. ☐ DELETION OF INVENTOR(S)
Signed Statement attached deleting inventor(s)
named in the prior application, see 37 CFR
1.63(d)(2) and 1.33(b).

5. ☒ Incorporation By Reference (useable if Box 4c is checked)
The entire disclosure of the prior application, from which a copy of the
oath or declaration is supplied under Box 4c, is considered as being
part of the disclosure of the accompanying application and is hereby
incorporated by reference therein.

6. ☐ Microfiche Computer Program (Appendix)

7. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)

a. ☐ Computer Readable Copy

b. ☐ Paper Copy (identical to computer copy)

c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☐ Assignment Papers (cover sheet & document(s))

9. ☐ 37 CFR 3.73(b) Statement ☐ Power of Attorney
(when there is an assignee)

10. ☐ English Translation Document (if applicable)

11. ☒ Information Disclosure Statement (IDS)/PTO-1449 ☒ Copies of IDS Citations

12. ☒ Preliminary Amendment

13. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)

14. ☐ Small Entity Statement(s) ☐ Statement filed in prior application
Status still proper and desired

15. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)

16. ☐ Other: _____

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior application No. 08/999,132

18. CORRESPONDENCE ADDRESS

☒ Customer Number or Bar Code Label

05514

(Insert Customer No. or Attach bar code label here)

or ☐ Correspondence address below

NAME

Address

City

State

Zip Code

Country

Telephone

Fax

+

CLAIMS	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS (37 CFR 1.16(c))	93-20 =	73	X \$ 18.00 =	\$1,314.00
	INDEPENDENT CLAIMS (37 CFR 1.16(b))	7-3 =	4	X \$ 78.00 =	\$312.00
	MULTIPLE DEPENDENT CLAIMS (if applicable) (37 CFR 1.16(d))			\$260.00 =	\$00.00
				BASIC FEE (37 CFR 1.16(a))	\$690.00
			Total of above Calculations =		\$2,316.00
	Reduction by 50% for filing by small entity (Note 37 CFR 1.9, 1.27, 1.28).				
	TOTAL =				\$2,316.00

19. Small entity status

- a. ☐ A Small entity statement is enclosed
- b. ☐ A small entity statement was filed in the prior nonprovisional application and such status is still proper and desired.
- c. ☐ Is no longer claimed.

20. ☒ A check in the amount of \$ 2,316.00 to cover the filing fee is enclosed.

21. ☐ A check in the amount of \$ _____ to cover the recordal fee is enclosed.

22. The Commissioner is hereby authorized to credit overpayments or charge the following fees to Deposit Account No. 06-1205:

- a. ☒ Fees required under 37 CFR 1.16.
- b. ☒ Fees required under 37 CFR 1.17.
- c. ☐ Fees required under 37 CFR 1.18.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

NAME	Elizabeth F. Holowacz
SIGNATURE	<i>Elizabeth F. Holowacz</i> 42,667
DATE	August 11, 2000

EFH:meg

NY_MAIN 103368 v 1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
: Examiner: S. Mulpuri
KATSUMI NAKAGAWA, ET AL.)
: Group Art Unit: 2812
Div. of Appln. No.: 08/999,132)
:
Filed: Herewith)
:
For: METHOD OF PRODUCING)
SEMICONDUCTOR MEMBER :
AND METHOD OF)
PRODUCING SOLAR CELLS : August 11, 2000

Assistant Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to examination on the merits in the above-identified divisional application, please amend the application as follows.

In the Specification:

At page 26,

Line 6, "609" should read --409--; and

Line 16, "607 and 612" should read --407 and

412--.

In the Claims:

Please cancel claims 4, 9, 24 and 68-81 without prejudice or disclaimer.

Please amend claims 1, 21, 29, 34, 41 and 42 as follows:

1. (Amended) A method of producing a semiconductor member[,] comprising the steps of:

forming a porous layer in a surface region of a first substrate;

forming a semiconductor layer on the porous layer by liquid phase epitaxy using a melting solution in which elements for forming the semiconductor layer to be grown are dissolved up to a supersaturated state or a substantially supersaturated state;

bonding a second substrate to a surface of the semiconductor layer opposite to a semiconductor layer surface bonded to the first substrate; and

separating the first substrate from the semiconductor layer by utilizing the porous layer to transfer the semiconductor layer to the second substrate.

21. (Amended) A method of producing a solar cell[,] comprising the steps of:

forming a porous layer in a surface region of a first substrate;

forming a semiconductor layer on the porous layer by liquid phase epitaxy using a melting solution in which elements for forming the semiconductor layer to be grown are dissolved up to a supersaturated state or a substantially supersaturated state;

bonding a second substrate to a surface of the semiconductor layer opposite to a semiconductor layer surface bonded to the first substrate; and

separating the first substrate from the semiconductor layer by utilizing the porous layer to transfer the semiconductor layer to the second substrate.

29. (Amended) A method [according to claim 21,] of producing a solar cell comprising the steps of:

forming a porous layer in a surface region of a first substrate;

forming a semiconductor layer on the porous layer by liquid phase epitaxy;

bonding a second substrate to a surface of the semiconductor layer opposite to a semiconductor layer surface bonded to the first substrate; and

separating the first substrate from the semiconductor layer by utilizing the porous layer to transfer the semiconductor layer to the second substrate;

wherein the liquid phase epitaxy includes that a melting solution in which elements for forming the semiconductor layer to be grown are dissolved [upto] up to a desired concentration is used and the melting solution is brought in contact with a surface of the porous layer while a surface temperature of the porous layer is made lower than a temperature at which elements in the melting solution having the desired concentration are saturated.

34. (Amended) A method according to claim 33, further comprising a step of separating [thed] the second substrate to transfer the semiconductor layer onto the third substrate.

41. (Amended) A method according to claim 21, wherein before the bonding of the second substrate, an impurity is introduced into the semiconductor layer.

42. (Amended) A method according to claim 21, wherein before the bonding of the second substrate, an impurity is introduced into the semiconductor layer to form a p-n junction.

Please add new claims 87-108 as follows:

--87. A method according to claim 29, wherein the semiconductor layer is formed on the porous layer, the semiconductor layer comprising a region formed by vapor phase epitaxy and a region formed by liquid phase epitaxy in this order.

88. A method according to claim 29, further comprising a step of removing the porous layer remaining on the surface of the first substrate after the first substrate is separated from the semiconductor layer.

89. A method according to claim 29, wherein the liquid phase epitaxy is conducted under a reducing atmosphere.

90. A method according to claim 29, wherein the liquid phase epitaxy includes that a melting solution in which elements for forming the semiconductor layer to be grown are dissolved is brought in contact with the porous layer.

91. A method according to claim 29, wherein the liquid phase epitaxy includes that a melting solution in which elements for forming the semiconductor layer to be grown are dissolved is brought in contact with an epitaxial layer formed on the porous layer.

92. A method according to claim 91, wherein the epitaxial layer is formed by vapor phase epitaxy.

93. A method according to claim 87, wherein the vapor phase epitaxy is conducted by decomposing a source gas while supplying a gas for forming a reducing atmosphere.

94. A method according to claim 29, wherein the bonding step of the second substrate is conducted using an adhesive.

95. A method according to claim 94, wherein the adhesive includes a water-soluble adhesive.

96. A method according to claim 29, further comprising a step of providing a third substrate on a separate surface for transferring the semiconductor layer onto the second substrate.

97. A method according to claim 96, further comprising a step of separating the second substrate to transfer the semiconductor layer onto the third substrate.

98. A method according to claim 29, wherein the second substrate has a water permeability.

99. A method according to claim 97, wherein the separation of the second substrate is conducted by the deterioration of adhesion of the adhesive used for bonding of the second substrate.

100. A method according to claim 99, wherein the deterioration of the adhesion is conducted by a liquid that has passed through the second substrate.

101. A method according to claim 99, wherein the adhesive is water-soluble, and the deterioration of the adhesion is conducted by a water that permeates the second substrate.

102. A method according to claim 29, wherein an impurity in the porous layer is diffused into the semiconductor layer.

103. A method according to claim 29, wherein the liquid phase is conducted with indium as a solvent.

104. A method according to claim 29, wherein before the bonding of the second substrate, an impurity is introduced into the semiconductor layer.

105. A method according to claim 29, wherein before the bonding of the second substrate, an impurity is introduced into the semiconductor layer to form a p-n junction.

106. A method according to claim 29, wherein the second substrate has an electroconductive surface.

107. A method according to claim 29, further comprising a step of removing the porous layer remaining on the transferred semiconductor layer.

108. A method according to claim 29, further comprising a step of forming an electrode on the transferred semiconductor layer.

109. A method according to claim 29, further comprising a step of introducing an impurity into the transferred semiconductor layer.

110. A method according to claim 29, further comprising a step of forming a semiconductor layer containing an impurity on the transferred semiconductor layer.--

Remarks

The claims are 1-3, 5-8, 10-23, 25-67 and 82-110, with claims 1, 21, 29, 52, 57, 82 and 85 being independent. Claims 4, 9, 24 and 68-81 have been cancelled without prejudice. Claims 1, 21, 29, 34, 41 and 42 have been amended. New claims 87-110 have been added. Reconsideration of the present claims is respectfully requested.


The specification has been amended in order to correct minor errors and to be consistent with the parent application to this divisional case.

Claims 1, 21, 29, 34, 41 and 42 have been amended. Claims 1 and 21 have been amended to incorporate the limitations of cancelled claims 4 and 24, respectively. Claim 29 has been rewritten in independent form. Claims 34, 41 and 42 have been amended to correct typographical errors. No new matter has been added.

New claims 87-110 have been added. Each of these claims depend ultimately from newly independent claim 29 and correspond to original claims 22, 23, 25-28 and 30-47, respectively. No new matter has been added.

Applicants' undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our below listed address.

Respectfully submitted,


Attorney for Applicants
Registration No. 42,607

FITZPATRICK, CELLA, HARPER & SCINTO
30 Rockefeller Plaza
New York, New York 10112-3801
Facsimile: (212) 218-2200

METHOD OF PRODUCING SEMICONDUCTOR MEMBER AND
METHOD OF PRODUCING SOLAR CELL

BACKGROUND OF THE INVENTION

5 Field of the Invention

The present invention relates to a method of producing a semiconductor member and a method of producing a solar cell. More particularly, the present invention relates to a method of producing a
10 semiconductor member comprising a thin film crystal formed on an inexpensive substrate and a method of producing a solar cell with high performance by using the semiconductor member.

Related Background Art

15 There have been extensively researched a solar cell as a power supply which is systematically coupled with a driving energy source of various equipments or a commercial power. The solar cell is so desired that a device can be formed on an inexpensive substrate to
20 comply with a cost demand. On the other hand, there has been normally employed silicon as semiconductor constituting the solar cell. In particular, from the viewpoint of the efficiency of converting a light energy into an electric power, that is, from the
25 viewpoint of the photoelectric conversion efficiency, single-crystal silicon is very excellent. On the other hand, from the viewpoint of increase in area and

reduction in costs, an amorphous silicon is advantageous. Also, in recent years, for the purpose of obtaining the low costs as low as amorphous silicon and high energy conversion efficiency as high as
5 single-crystal, polycrystal silicon has become used.

However, in single-crystal or polycrystal silicon, since a lump-shaped crystal is sliced into a plate-shaped substrate, it is difficult to make its thickness 0.3 mm or less. Thus, the material used for the
10 substrate has not been effectively utilized because the substrate generally has a thickness much over a thickness necessary for absorbing an incident light (20 μm to 50 μm). Also, in recent years, there has been proposed a method of forming a silicon sheet by using a
15 spin method in which a liquid droplet of melted silicon is allowed to flow into a die. Even in this method, the thickness of the substrate is about 0.1 to 0.2 mm at the minimum, which is not sufficiently thinned. In other words, there is a room for more reducing the
20 costs by further thinning silicon.

To achieve the above, there has been proposed an attempt of achieving high energy conversion efficiency and low costs of a solar cell in which a thin epitaxial layer grown on a single-crystal silicon substrate is
25 separated (peeled) from the substrate (Milnes, A.G. and Feucht, D.L., "Peeled Film Technology Solar Cells", IEEE Photovoltaic Specialist Conference, p. 338, 1975).

In this method, an intermediate layer of SiGe is interposed between single-crystal silicon for forming the substrate and the grown epitaxial layer, and a silicon layer is allowed to (hetero) epitaxially grow thereon. Therefore, the intermediate layer is selectively melted so that the growth layer is peeled off. However, in general, the hetero-epitaxially grown layer is liable to have defects induced on a growth interface because the layer is different in lattice constant from the substrate. Also, this method is not advantageous in the process costs because of use of a material such as germanium which is remarkably expensive more than silicon.

Also, U.S. Patent No. 4,816,420 discloses that a thin crystal solar cell is obtained by making selective epitaxial growth on a crystal substrate through a mask material, forming sheet-like crystal by using a method of allowing crystal to laterally grow, and thereafter separating the crystal from the substrate. However, in this method, since the sheet-like crystal is mechanically peeled off using cleavage, the sheet-like crystal is liable to be damaged during a peel-off process when the crystal has a certain size or more. In particular, in the case of increasing the area of the crystal as in the solar cell, it becomes difficult to practically employ the above method.

Also, Japanese Patent Application Laid-Open No.

6-45622 discloses that after a porous silicon layer is formed in the surface region of a silicon wafer surface by anodization, the porous layer is peeled off from the wafer, and after the peeled porous layer is fixed onto a metal substrate, an epitaxial layer is formed on the porous layer, to thereby fabricate a thin-film crystal solar cell by using this. However, in this method, since the metal substrate is exposed to a high-temperature process, impurities are liable to be mixed into the epitaxial layer, which leads to a problem that the characteristic is restricted. Also, as realized in the amorphous silicon solar battery, if a thin semiconductor layer is formed on a flexible substrate, for example, a film of polymer such as polyimide, it can be located on a substance having a curved surface, thus expecting the enlargement of an applied field. However, because a high temperature is required in a process of the above-mentioned single-crystal or polycrystal silicon solar cell, it is difficult to use a substrate having poor heat resistance at a high temperature.

By the way, Japanese Patent Application Laid-Open No. 8-213645 discloses that an active layer of the solar cell is allowed to epitaxially grow on amorphous silicon formed in the surface region of a silicon wafer by anodization, and thereafter the active layer can be peeled off from a portion of the porous silicon layer.

Therefore, not only the expensive single-crystal substrate can be repeatedly utilized, but also a high-efficiency solar cell can be formed on a flexible low-heat-resistant substrate. However, according to the disclosure of Japanese Patent Application Laid-Open No. 8-213645, the epitaxial growth of the active layer is conducted by the CVD method. In the CVD method, a source gas such as dichlorosilane (SiH_2Cl_2) or trichlorosilane (SiHCl_3) and a large amount of hydrogen gas are used. When a silicon film is deposited to 20 to 50 μm in thickness by using a large amount of the expensive gas, it is correspondingly expensive and considerably disadvantageous from the viewpoint of the costs in comparison with amorphous silicon which is required to be deposited to at most 0.5 to 1.0 μm in thickness.

SUMMARY OF THE INVENTION

The present invention has been made in view of the above circumstances, and therefore an object of the present invention is to provide a method of producing a semiconductor member excellent in characteristics and a method of producing a solar cell by using the semiconductor member.

Another object of the present invention is to provide a method of producing a semiconductor member in which crystal semiconductor excellent in various

characteristics can be formed even on a substrate having no high-temperature resistant property and a method of producing a solar cell by using the semiconductor member.

5 Still another object of the present invention is to provide a method of producing a semiconductor member in which crystal semiconductor excellent in various characteristics can be formed even on a flexible substrate and a method of producing a solar cell by
10 using the semiconductor member.

 A further object of the present invention is to provide a method of producing a semiconductor member which can be variously applied, used and arranged and a
15 method of producing a solar cell by using the semiconductor member.

 A still further object of the present invention is to provide a method of producing a semiconductor member having excellent semiconductor characteristics at low costs and a method of producing a solar cell having
20 various characteristics such as excellent photoelectric conversion characteristics or use characteristics at low costs by using the semiconductor member.

 A still further object of the present invention is to provide a method of producing a solar cell which can
25 exhibit high conversion efficiency.

 A still further object of the present invention is to provide a semiconductor member which can be obtained

by peeling off an epitaxial layer formed on a crystal substrate from the crystal substrate while reusing the crystal substrate, to provide a semiconductor member having high performance at low costs by use of an inexpensive raw material, and to provide a solar cell which is formed by using the semiconductor member while reusing the crystal substrate, and which has high performance, at low costs by use of an inexpensive raw material.

10 In order to achieve the above objects, according to the present invention, there is provided a method of producing a semiconductor member or a solar cell, the method comprising the steps of:

forming a porous layer in a surface region of a first substrate;

forming a semiconductor layer on the porous layer by liquid phase epitaxy;

20 bonding a second substrate to a surface of the semiconductor layer opposite to a semiconductor layer surface bonded to the first substrate; and

separating the first substrate from the semiconductor layer by utilizing the porous layer to transfer the semiconductor layer to the second substrate.

25 Also, according to the present invention, there is provided a method of producing a semiconductor member, the method comprising the steps of:

(a) forming a porous layer in a surface region of a first substrate;

(b) immersing the porous layer into a melting solution in which elements for forming a semiconductor layer to be grown is dissolved up to a supersaturated state or a substantially supersaturated state under a reducing atmosphere to grow a semiconductor layer on a surface of the porous layer;

(c) bonding a second substrate to a surface side of the first substrate on which at least the porous layer and the semiconductor layer are formed; and

(d) separating the first substrate from the second substrate at the porous layer to transfer the semiconductor layer separated from the first substrate to the second substrate.

Further, according to the present invention, there is provided a method of producing a semiconductor member, the method comprising the steps of:

(a) forming a porous layer in a surface region of a first substrate;

(b) immersing, into a melting solution in which elements for forming a semiconductor layer to be grown is dissolved up to a desired concentration, the porous layer whose surface temperature is made lower than a temperature at which the melting solution having the desired concentration is saturated, to grow a semiconductor layer on a surface of the porous layer;

(c) bonding a second substrate onto a surface side of the first substrate on which at least the porous layer and the semiconductor layer are formed; and

(d) separating the first substrate from the second substrate at the porous layer to transfer the semiconductor layer separated from the first substrate to the second substrate.

In addition, according to the present invention, there is provided a method of producing a semiconductor member, the method comprising the steps of:

(a) forming a porous layer in a surface region of a first crystalline substrate;

(b) growing a first thin-film semiconductor layer on a surface of the porous layer in vapor phase by decomposing a source gas;

(c) immersing the first thin-film semiconductor layer into a melting solution in which elements for forming a second thin-film semiconductor are dissolved up to a saturated state or a supersaturated state under a reducing atmosphere to grow a second thin-film semiconductor layer of a conductive type different from that of the first thin-film semiconductor layer on a surface of the first thin-film semiconductor layer in liquid phase;

(d) bonding a second substrate onto a surface of the second thin-film semiconductor layer or onto a surface of a layer further formed on the second thin-

film semiconductor layer;

(e) separating the first thin-film semiconductor layer from the first substrate by exerting a force on the porous layer to transfer the first thin-film semiconductor layer to the second substrate.

Yet still further, according to the present invention, there is provided an apparatus of producing a semiconductor member or a solar cell in which a substrate comprising a porous layer is stored and a semiconductor layer is formed on the porous layer, the apparatus comprising:

a liquid phase growth vessel for immersing a first thin-film semiconductor layer into a melting solution in which elements for forming a second thin-film semiconductor layer are dissolved up to a saturated state or a supersaturated state under a reducing atmosphere to grow a second thin-film semiconductor layer on a surface of the first thin-film semiconductor layer in liquid phase; and

means for conveying the substrate between a vapor phase growth vessel and the liquid phase growth vessel while keeping the reducing atmosphere.

In the above method, it is preferable that the semiconductor layer is formed on the porous layer so that the semiconductor layer comprises a region formed by vapor phase epitaxy and a region formed by liquid phase epitaxy in this order.

Also, the above method may further comprise a step of removing the porous layer remaining on the surface of the first substrate after being separated from the semiconductor layer.

5 Further, it is desirable that the liquid phase epitaxy is conducted by using a melting solution in which elements for forming the semiconductor layer to be grown are dissolved up to a supersaturated state or a substantially supersaturated state.

10 In addition, it is preferable that the liquid phase epitaxy is conducted under a reducing atmosphere.

 Furthermore, it is preferable that the liquid phase epitaxy includes that a melting solution in which the elements for forming the semiconductor layer to be
15 grown are dissolved is brought in contact with the porous layer.

 Yet still further, it is preferable that the liquid phase epitaxy includes that a melting solution in which the elements for forming the semiconductor
20 layer to be grown are dissolved is brought in contact with an epitaxial layer formed on the porous layer.

 Yet still further, it is desirable that the epitaxial layer is formed by vapor phase epitaxy.

 Yet still further, it is preferable that the
25 liquid phase epitaxy includes that a melting solution in which elements for forming the semiconductor layer to be grown is used and the melting solution is brought

in contact with the surface of the porous layer while a surface temperature of the porous layer is made lower than a temperature at which the elements in the melting solution having the desired concentration are saturated.

Yet still further, it is desirable that the vapor phase epitaxy is conducted by decomposing a source gas while supplying a gas for forming a reducing atmosphere.

Yet still further, the step of bonding the second substrate may be conducted using an adhesive. In this situation, the adhesive includes a water-soluble adhesive.

Yet still further, there may be provided a third substrate on a separate surface for separating and transferring the semiconductor layer to the second substrate. In this situation, the second substrate may be separated so that the semiconductor layer is transferred to the third substrate.

Yet still further, the second substrate may have a water permeability. Also, the separation of the second substrate may be conducted by lowering of adhesion of the adhesive used for bonding of the second substrate. In this situation, it is desirable that the lowering of the adhesion is conducted by a liquid that has passed through the second substrate.

In addition, the impurities in the porous film may

be diffused into the semiconductor layer.

It is preferable that the liquid phase epitaxy is conducted with indium as a solvent.

Yet still further, in the above producing method,
5 it is preferable that prior to the formation of the semiconductor layer into which the impurities are introduced, a semiconductor layer into which no impurities are introduced or impurities are introduced with a low concentration is formed on the tread surface
10 of the first substrate after being subjected to a surface treatment by liquid phase growth.

Yet still further, in the above producing method, semiconductor having a purity of 99.99% or less may be used as the first substrate.

15 Yet still further, in the above producing method, the first substrate may be a crystalline one, and in particular may be a silicon single-crystal.

Yet still further, in the above apparatus, there may be provided a vapor phase growth vessel for
20 decomposing a source gas in the reducing atmosphere to grow the first thin-film semiconductor layer on the surface of the porous layer of the substrate in the vapor phase.

According to the present invention, epitaxial
25 growth is employed for providing a semiconductor member with higher performance and quality, and also for providing a solar cell with higher conversion

efficiency.

In order to perform the epitaxial growth of silicon at low costs, it is advantageous to use the liquid phase growth method rather than a method of using a gas such as the CVD method. In the liquid phase growth method, silicon grains are dissolved in a melted metal such as Sn, In, Cu or Al, a crystalline substrate is immersed therein, and silicon is allowed to grow on the substrate in a state where the solution is made supersaturated state. The liquid phase growth method is expensive in the raw material to be used, and the raw material to be wasted is reduced. Also, since the growth is conducted at a very low temperature in comparison with the melting point of Si such as 100°C or lower, the liquid phase growth method is advantageous more than the spin method from the viewpoint of an energy. However, when silicon growth is conducted by using the liquid phase growth method in fact, there are not less cases, under the existing circumstances, in which the grown silicon cannot withstand use as the solar cell because of the problem that abnormal crystal grains are grown, or the grown thin-film semiconductor layer cannot be well separated. Therefore, it is normally difficult to accomplish both of high performance as single-crystal or polycrystal and low costs as much as amorphous silicon.

Also, as the substrate (first substrate) for

epitaxial growth, there can be used for not only a single-crystal silicon wafer but also a high-quality polycrystal silicon wafer. However, in order to prevent an influence of impurity diffusion from the substrate, there is required high purity of the substrate such that a device is made in the substrate itself. Therefore, from the viewpoint of the costs, it is desirable that the use of the substrate can be repeated at least several tens times. However, as the number of times of repeated use is increased, the anodization condition is varied depending on a variation of the surface state of crystal, etc., thereby making producing management difficult.

Taking the above circumstances into consideration, embodiments of the present invention will be described referring to a solar cell as an example. The present invention utilizes a process of transferring a semiconductor layer to a second substrate. Since on the semiconductor layer of the present invention can be formed a semiconductor device such as a transistor, a diode or an LED as occasion demands, the present invention is not particularly limited to the production of the solar cell.

An example of the structure of a solar cell produced according to the method of the present invention is shown in a schematic cross-sectional views of Fig. 1, and a preferred example of producing steps

according to the present invention is shown in schematic cross-sectional views of Figs. 2A to 2I, respectively. In Figs. 1 and 2A to 2I, reference numeral 105 and 205 denote substrates; 109 and 209, back-surface electrodes; 104 and 204, p^+ (or n^+) type layers; 103 and 203, active p^- (or n^-) type layers; 106 and 206, n^+ (or p^+) type layers; 107 and 207, transparent conductive layers; and 108 and 208, collecting electrodes. In this example, the n^+ (or p^+) type layers 106, 206 and the active p^- (or n^-) type layers 103, 203 form a semiconductor junction to produce a photoelectromotive force. The active p^- (or n^-) type layers 103 and 203 are main bodies which absorb a solar light to generate carriers and are thickened to about 10 to 50 μm in case of silicon. On the other hand, the n^+ (or p^+) type layers 106 and 206 is sufficiently thickened to 1 μm or less. Also, the p^+ (or n^+) type layers 104 and 204 form a back-surface field between the electrodes 109, 209 and the layers 104, 204 and provide a function of preventing re-bonding of the carriers in the vicinity of the electrodes 109 and 209 although it is not essential. Also, they sufficiently functions with the thickness of 1 μm or less. In this example, the expressions of the n^+ (or p^+) type layers 106 and 206, the active p^- (or n^-) type layers 103 and 203, and the p^+ (or n^+) type layers 104 and 204 mean that if the layers 106 and 206 are of

n⁺-type, the layers 103 and 203 are of p⁻-type, and the layers 104 and 204 are of p⁺-type, whereas if the layers 106 and 206 are of p⁺-type, the layers 103 and 203 are of n⁻-type, and the layers 104 and 204 are of n⁺-type.

5 Thus, these layers function with the combination of the respective conductive types, in one combination containing the layers 106 and 206 of n⁺-type, the collecting electrode side generates a negative electromotive force, whereas in the combination
10 containing the layers 106 and 206 of p⁺-type, the collecting electrode side generates a positive electromotive force.

Subsequently, an outline of producing steps according to the present invention will be described
15 with reference to Figs. 2A to 2I. For example, a single-crystal semiconductor wafer is used as a first substrate 201 of crystalline. Impurities are thermally diffused, ions are implanted into the surface of the first substrate 201, or impurities are introduced when
20 producing the wafer to make at least the wafer surface p⁺ (or n⁻) type (Fig. 2A). Then, the wafer surface on the side where the impurities are introduced is anodized in a HF solution to form a porous layer 202 (Fig. 2B). In the porous structure formation by
25 anodization, as disclosed in Japanese Patent Application Laid-Open No. 7-302889, an anodization current level is, for example, changed from a low level

to a high level on the way in such a manner that a porosity change is given of the structure of the porous layer in advance, thereby being capable of controlling such that the substrate and the semiconductor layer are

5 liable to be separated from each other at the porous layer after epitaxial growth. Subsequently, a single-crystal semiconductor layer 203 that functions as the active p^- (or n^-) type layer is allowed to epitaxially grow on the porous layer by the liquid phase growth

10 method. Then, as occasion demands, a single-crystal semiconductor layer 204 of the p^+ (or n^+) type layer is allowed to epitaxially grow. Moreover, a second substrate 205 on which a back-surface electrode 209 is formed is bonded onto the single-crystal semiconductor

15 layer 204, or after the single-crystal semiconductor layer 204 is formed, the back-side electrode 209 is formed on the single-crystal semiconductor layer 204, and then the second substrate 205 is bonded thereonto (Figs. 2D to 2E). A force is exerted between the

20 bonded second substrate 205 and the first crystalline substrate 201 to mechanically separate the porous layer, thereby transferring the single-crystal semiconductor layers 203 and 204 from the first crystalline substrate 201 to the second substrate 205

25 (Fig. 2F). After transfer, the porous layer 202a remaining on the surface of the single-crystal semiconductor member 203 is removed by etching, an

n⁺ (or p⁺)-type semiconductor layer 206, a transparent conductive layer 207 and a collecting electrode 208 are formed to complete a solar cell (Figs. 2G to 2H). A porous layer 202b remaining on the surface of the first crystalline substrate 201 after the completion of
5 separation is removed and treated by etching, etc., and the first crystalline substrate is then again subjected to the first step (Fig. 2A).

Then, the producing method according to the
10 present invention will be described in more detail.

First, an example of using silicon as the material of the first substrate 201 of crystalline as to the porous layer 202 (that is, an example in which the porous layer is made of silicon) will be described.
15 The mechanical strength of the silicon porous layer 202 is considered to be sufficiently weaker than bulk silicon although it depends on the porosity. For example, if the porosity is 50%, the mechanical strength is regarded to be half of the bulk or less.
20 When the second substrate 205 is allowed to bond onto the surface of the porous silicon layer 202, if a sufficient adhesion is exerted between the second substrate 205 and the porous layer 202, the porous silicon layer 202 is destroyed by applying a
25 compression, a tensile force or a shearing force between silicon wafer 201 and the second substrate 205 where the porous layer is formed. If the porosity is more

increased, the porous layer 202 can be destroyed with a weaker force.

The silicon substrate can be made porous by the anodization method using an HF solution 10% or more in concentration. A amount of current that flows at the time of the anodization is appropriately in a range of about several to several tens mA/cm² although being appropriately determined depending on the HF concentration, a desired thickness of the porous layer, the surface state of the porous layer or the like. Also, by addition of alcohol such as ethyl alcohol to the HF solution, bubbles of the reactive gas which is generated at the time of the anodization can be removed from a surface to be reacted without being stirred, thereby being capable of forming the porous silicon uniformly and efficiently. The amount of alcohol to be added is appropriately determined depending on the HF concentration, a desired thickness of the porous layer, the surface state of the porous layer or the like. In particular, attention has been paid to prevent the HF concentration from being too lowered. The density of the single-crystal silicon is 2.33 g/cm³, whereas the density of the porous silicon layer is varied by varying the concentration of the HF solution in a range of 50 to 20% to be in a range of 1.1 to 0.6 g/cm³. Also, the porosity can be varied by a variation of the anodization current. When the current increases, the

porosity also increases more.

Positive holes are required for anodic reaction in formation of the porous silicon by the anodization.

For that reason, silicon is made porous using p-type

5 silicon in which positive holes mainly exist (T.

Unagami, J. Electrochem. Soc., vol. 127,476 (1980)).

However, on the other hand, there has been reported

that even a low-resistant n-type silicon is made porous

(R.P Holmstrom and J.Y. Chi, Appl. Phys. Lett., vol.

10 42,386 (1983)). Thus, the low-resistant silicon can be

made porous regardless of the kind of p-type or n-type.

Also, silicon can be selectively made porous depending

on the conductive type so that only the p-type layer

can be made porous by conducting the anodization in a

15 dark place as in the FIPOS (Full Isolation by Porous

Oxidized Silicon) method.

The porous silicon obtained by subjecting the

single-crystal silicon to anodization has pores having

a diameter of about several nm formed according to the

20 observation using a transmission electromicroscope, and

its density becomes half of the single-crystal or less.

Even in that fact, monocrystallinity is maintained,

thereby being capable of allowing an epitaxial layer to

grow on the porous silicon. Also, because the porous

25 layer has a large number of pore spaces formed inside

thereof, the surface area is remarkably increased in

comparison with the volumn. Aas a result, a chemical

etching rate of the porous layer is remarkably accelerated in comparison with the etching rate of the normal single-crystal layer. Further, there has been known that an excellent epitaxial layer is obtained by
5 annealing at 950 to 1,100°C in a hydrogen atmosphere prior to epitaxial growth. It is presumed that this is because the outermost surface of the porous layer is reconstructed and flattened at a high temperature in a reducing atmosphere (Nikei Micro Device, July of 1994,
10 p. 76).

Similarly, the porous layer is obtained by anodization when single-crystal silicon is replaced by polycrystal silicon, and a crystal silicon layer can grow on the porous layer of polycrystal silicon (in
15 this case, partial epitaxial growth corresponding to a size of crystal grains of the polycrystal silicon is enabled). The more details will be described with reference to various Examples as described below.

Then, the liquid phase growth method for forming
20 the thin-film semiconductor layer will be described. Fig. 3 is a schematic diagram for explanation of the liquid phase growth method in the producing method of the present invention in a thermal equilibrium state of solvent M and solute S (for example, silicon). In the
25 figure, a horizontal axis 501 represents a mean concentration of the solute S in the solution (or apparent concentration depending on circumstances),

where a left end thereof represents the state of a pure solvent, and the concentration of the solute S increases toward the right side. Also, a vertical axis 502 represents a temperature of the solution, and the state of the solution is roughly classified into two regions with a curve 503 as its boundary. Also, at a position P in a region 504, the solute S is uniformly dissolved in the solvent M, and its concentration is coincides with the concentration as indicated by the horizontal axis. In a region 505, a part of the solute S is solidified and deposited, and for example, a solid S and the solution having a concentration Dq exist together at a position Q. A substrate made of a material which is not dissolved at a temperature of a state R0 on the curve 503 is immersed in the solution in the state R0, and as the temperature of the solution gradually decreases, the concentration of the solute S in the solution is reduced along the curve 503, for example, up to R1. The solute S corresponding to a difference in concentration between R0 and R1 is deposited on the surface of the substrate as solid. In particular, in the case where the substrate is crystalline, there is a case where the solid S also becomes crystalline according to the crystallinity of the substrate, which is called "epitaxial growth". Normally, when the material of the substrate and the solid S are the same, the epitaxial growth is most

facilitated. However, even if they are different in material, the epitaxial growth is enabled (hetero-epitaxial growth). In this way, the thin film semiconductor can be allowed to grow on the surface of the first substrate of crystalline. In general, after the substrate is immersed into the solution which is made just a saturated state or which is made a slightly unsaturated state for a very short time and then is adjusted to the saturate state, the growth of crystal starts. It is presumed that in the above manner, the impurities and the defects are removed from the surface of the substrate by the thermal equilibrium effect, and crystal with high quality is liable to grow. However, it has been proved that there arise some problems when crystal is actually allowed to grow on the porous layer by the liquid phase growth method. Hereinafter, a description will be given on the basis of the experiments which have been conducted by the present inventors.

The epitaxial growth is enabled by methods other than the liquid phase growth method, such as a method of conducting the epitaxial growth by decomposing a gas such as silane (SiH_4), dichlorosilane (SiH_2Cl_2) or trichlorosilane (SiHCl_3) by heat or the action of plasma (CVD method). However, since the liquid phase growth method conducts crystal growth in a state nearest to the thermal equilibrium state, a high-quality thin film

semiconductor layer is readily obtained, and also a material necessary for deposition is low in costs.

First, Fig. 4 shows a schematically structural cross-sectional view of a suitable apparatus for growing a semiconductor layer for a solar cell according to the present invention. This apparatus is used in Experimentals 1 to 3 and Example 1.

As shown in Fig. 4, the entire apparatus is roughly classified into three sections. Reference numeral 401 denotes a load lock chamber whose interior can be air-tightly kept by closing an open/close door 402. Reference numeral 403 denotes a nitrogen introduction line which can replace atmosphere in the chamber 401 by nitrogen. Reference numeral 404 denotes a hydrogen annealing vessel or a vapor phase growth vessel, and a sample can be conveyed between the vessel 404 and the load lock chamber 401 through a gate valve 405. Hydrogen or source gases for forming a film can be introduced to the hydrogen annealing vessel 404 from the hydrogen introduction line 406 while controlling the flow rate of hydrogen or source gases. Reference numeral 408 denotes a heater for heating substrates 416 which is located inside of the vessel 404. The substrates 416 each comprising a pair of two silicon wafers bonded to each other are arranged such that each of a plurality of the substrates 416 is in parallel to one another while a certain interval is kept between

the substrates by a holder. The substrates can be vertically conveyed through a gate valve by a conveying mechanism not shown in the drawing. Reference numeral 409 denotes a liquid phase growth vessel, and a sample
5 can be conveyed between the hydrogen anneal vessel 404 and the liquid phase growth vessel 609 through the gate valve 410. Hydrogen is supplied to the liquid phase growth vessel 409 from the hydrogen introduction line 411 so that atmosphere can be kept to a reduction state
10 during liquid phase growth. Reference numeral 414 denotes a carbon boat which is heated by the heater 413 in such a manner that elements for forming a semiconductor layer such as silicon and dopant elements as occasion demands are dissolved in a low-melting-
15 point metal such as In which exists inside of the carbon boat 414. Reference numerals 607 and 612 denote gas exhaust tubes, and 615 is a melting material.

(Experiment 1)

After a p-type silicon wafer, as a substrate, on a
20 surface of which a porous layer was formed by a standard anodization, was held in a hydrogen air flow at a substrate surface temperature (T_{surf}) of $1,050^{\circ}\text{C}$ for 30 minutes (after annealing), a temperature went down to 900°C . On the other hand, silicon was
25 dissolved into a metal indium solvent at a solvent temperature (T_m) of 900°C up to a concentration with which the solvent was just saturated. Thereafter, a

p-type silicon wafer on a surface of which a porous layer was formed by the standard anodization was immersed in the solvent at the surface temperature T_{surf} of 900°C , and then was gradually cooled at a cooling rate of $-1^{\circ}\text{C}/\text{min}$. As a result, a silicon layer was deposited on the surface of the silicon wafer. However, an uneven structure was found on the surface, and also a discontinuous ring-shaped RHEED (reflection high energy electron diffraction) image was obtained. Therefore, it was found that the grown silicon was irregular polycrystal. In addition, when attempt was made to separate that film, there was a part of the film which remained without being separated and the film could not be used for the solar cell. However, when crystal growth is conducted on the porous layer having the same condition by the thermal CVD method using dichlorosilane, there is obtained a single-crystal film with excellent smoothness. Also, the entire film can be completely separated. On the other hand, a high-quality single-crystal is obtained similarly in the case where liquid phase growth is made on the same p-type silicon wafer under the same condition without any formation of the porous layer. In other words, it has been found that an inherent problem is generated when crystal is allowed to grow on the porous layer in the liquid phase.

(Experiment 2)

Silicon was dissolved in the metal indium at 900°C until it became just a saturated state. In other words, the temperature T_{sat} at which the solution was saturated was 900°C.

Then, after the temperature of the solvent was set to the values of T_m column in Table 1, a p-type silicon wafer on a surface of which a porous layer was formed by the standard anodization was annealed in the hydrogen air flow as in Experiment 1, and thereafter was immersed in the solvent while the substrate surface temperature was set to be equal to the temperature of the solvent ($T_{surf} = T_m$), and then is gradually cooled at a cooling rate of $-1^\circ\text{C}/\text{min}$ to deposit the thin-film silicon having a thickness of 20 μm . As a result, as indicated in Table 1, differences are found in RHEED image and separation state depending on T_m .

Table 1

T_m	RHEED IMAGE	SEPARATION
904°C	Piramid-like nonuniform growth	
902°C	Discontinuous film	
900°C	discontinuous ring image	non-separable
898°C	foggy spot image	substantially separable
896°C	foggy spot image	substantially separable
894°C	spot image	completely separable
892°C	spot image	completely separable

In this experiment, when T_m is lower than T_{sat} ,

the amount of silicon corresponding to an amount over the saturated concentration should be immediately deposited as in the point Q of Fig. 3. However, in fact, supersaturated silicon can exist in the solution within some range. The supersaturated state is unstable, and it is presumed that if a solid such as a wafer exists in the solution, silicon starts to be deposited on the wafer from the solution close to its surface.

In this way, it has been proved that the state of the thin film semiconductor is remarkably improved by immersing the silicon wafer after the solution is made in the saturated state to some degree. As a result of experiment while T_{sat} and T_m were varied, the present inventors have concluded that when a relationship of $T_{sat} - T_m \geq 5^\circ$ is substantially satisfied, crystallinity is particularly high, and a well separatable film can be grown. However, if the degree of supersaturated state is remarkable, the solute is immediately deposited from the solution, thereby not performing stable deposition.

The reason why the above result is obtained is presumed by the present inventors, as follows. That is, it is presumed that the solute atoms to be deposited and the solute atoms to be dissolved coexist on the surface of the wafer even in the state where the solute is deposited from the micro viewpoint, and

deposition is made when there are a large net amount of solute atoms to be deposited (in this point, it is considered that this method is different from the CVD method in which deposition occurs substantially in one way with chemical reaction of molecules from the vapor phase). Therefore, it is presumed that when net deposition is not made at an initial growth stage, or net deposition rate is low, because a large amount of atoms which are dissolved from the substrate exist, the initial substrate structure is changed with elapse of time. In particular, since the porous layer has a large effective surface area and a high reactivity, delivery of atoms between the substrate and the solute in the solution is frequently made so that the porous layer is liable to be remarkably modified. For that reason, it is presumed that crystallinity is lost or pores are embedded, thereby making it difficult to conduct separation in the following step.

Also, in the liquid phase growth method, it is said that in the initial substrate immersion stage, if the solution is not unsaturated, high-quality crystal cannot be grown. However, if the porous layer is located in a high-temperature reducing atmosphere, the surface defects are removed, and impurities such as oxygen are also removed. Therefore, it is considered from the above circumstances that high-quality crystal is more readily obtained in the case where the

solution is supersaturated from the initial.

(Experiment 3)

Silicon was dissolved in a metal indium solvent at 900°C until the solution had a concentration with which silicon was just saturated. A p-type silicon wafer on a surface of which a porous layer was formed by the standard anodization was annealed in the hydrogen air flow, and thereafter was immersed in the solvent while the substrate surface temperature was set to values of T_{surf} column shown in Table 2, and then was gradually cooled at a cooling rate of $-1^{\circ}\text{C}/\text{min}$ to deposit the thin-film silicon of $20\text{ }\mu\text{m}$ in thickness. It is presumed that the surface temperature of the substrate coincides with the temperature T_m of the solvent immediately after the silicon wafer is immersed in the solution.

Table 2

T_{surf}	RHEED IMAGE	SEPARATION
904°C	pyramid-like nonuniform growth	
902°C	discontinuous ring image	partially separatable
900°C	discontinuous ring image	non-separatable
898°C	foggy spot image	substantially separatable
896°C	foggy spot image	substantially separatable
894°C	spot image	completely separatable
892°C	spot image	completely separatable

It is presumed that although the metal indium solvent is not supersaturated in an initial growth stage, if $T_{surf} < T_{sat}$, preferably $T_{sat} - T_{surf} \geq 5^\circ$ is satisfied, adverse influence on the porous layer can
5 be substantially prevented. $T_{sat} = T_m = 900^\circ\text{C}$ is satisfied until cooling starts.

Then, the formation of a junction will be described. In Fig. 1, the p^+ (or n^+) type layer 104 (for back-surface field formation) on the substrate 105
10 side and the n^+ (or p^+) type layers 106 on the light incident side can grow by the liquid phase growth method separately from the active p^- (or n^-) type layer 103, respectively. For example, in the case where Ga is solvent, Ga is dissolved in the silicon film so that
15 it can be doped to become p^+ type. In the case where Sb is solvent, Sb is dissolved in the silicon film so that it can be doped to become n^+ type. In the case where In is solvent, since it is difficult to dissolve In in silicon, Ga is added to In so that it can be doped to
20 become p -type. Similarly, As is added to In so that it can be doped to become n -type.

Alternatively, the junction may be formed by thermal diffusion after a dopant diffusion source is coated or deposited on the surface of the active layer
25 103, or by implanting dopant atoms to the silicon layer by ion implantation.

Also, as already described, n^+ (or p^+) type layer

106 on the light incident side can be formed separately after the semiconductor thin film is separated. In the case of using a substrate having low heat resistance such as a resin film, there is the necessity of
5 applying a depositing method such as the plasma CVD by which deposition is enabled at a low temperature. The more details will be described with reference to Examples.

Subsequently, the first substrate of crystalline
10 and its reuse will be described with reference to Figs. 2A to 2I. As already described, in order to allow the thin film silicon crystal to grow, it is the best to use a silicon wafer as the first substrate. The entire silicon wafer may be doped to become p-type, or only
15 the surface of the silicon wafer may be doped to p-type in order to conduct anodization of a silicon wafer. As a method of achieving this, there are used measurements such as thermal diffusion or ion implantation. A p-type layer is made porous by anodization to produce a
20 porous layer 202.

Also, the porous layer 202a remaining on the active layer 203 which is separated from the silicon crystal substrate is selectively removed. Also, the porous layer 202b remaining on the surface of the
25 silicon crystal substrate from which the active layer 203 is separated is selectively removed for reuse. Only porous silicon can be chemically etched in an

electroless wet manner using at least one kind of a normal silicon etching solution, hydrofluoric acid which is a selective etching solution for porous silicon, a mixture solution in which at least any one of alcohol and hydrogen peroxide water is added to hydrofluoric acid, buffered hydrofluoric acid, and a mixture solution in which at least any one of alcohol and hydrogen peroxide water is added to buffered hydrofluoric acid.

10 The first substrate is gradually reduced in thickness as the separating step is repeatedly conducted. There is a tendency that roughness and defects on the surface of the silicon layer are gradually increased. The number of times where the silicon wafer can be repeatedly used is restricted by those factors. The number of times where the single-crystal wafer of expensive silicon can be used largely effects the costs. From the above viewpoint, several improvements can be made. That is, the thickness can be restored by conducting epitaxial growth. In this case, it is particularly a convenience to use the liquid phase growth method that enables growth at lower costs.

25 The above method has several advantages from the viewpoint of reducing the costs. That is, when the epitaxial layer is doped to become p-type during growing, a step of doping for p-type is not required.

Also, even when a silicon wafer having low quality such that the concentration of impurities is unstable is used, the reproducibility of the anodization step is improved to stabilize the quality of the porous layer.

5 Moreover, when the epitaxial layer non-doped or doped with a low concentration is deposited prior to a doping step of the surface for p-type, the reproducibility of the anodization can be further improved. Although the generation of roughness, etc., on the surface as it is
10 repeatedly used largely influences a post step, mechanical grinding can be conducted if required.

The above description was given provided that the thin film semiconductor is single-crystal. However, this is not essential. In the application of the
15 present invention to the solar cell, even when the thin film semiconductor is polycrystal, it is put in practical use as a solar cell having sufficiently high performance if the size of crystal grains is about 1 mm as a reference. Even if the first substrate of
20 crystalline is polycrystal, epitaxial growth is locally made within a range of the respective crystal grains, to thereby obtain polycrystalline thin film semiconductor layer. The more details will be described with reference to Examples.

25 In the solar cell according to the present invention, a polymer film is appropriately used as a low-heat-resistant substrate material to which the thin

film crystal semiconductor layer is transferred, and the representative material is polyimide film. Also, glass, a plastic plate made of resin or the like can be used. In the solar cell according to the present

5 invention, as a method of bonding the substrate to the thin film crystal semiconductor layer, there is appropriately used a method in which a conductive metal paste such as copper paste or copper paste is inserted between the substrate and the thin film crystal

10 semiconductor layer to bring them in close contact with each other, and then they are burned and adgered onto each other. In this case, metal such as copper or silver after being burned also functions as a back-surface electrode and a back-surface reflection layer.

15 Also, in case of a substrate such as the polymer film, the substrate and the thin film crystal semiconductor layer may be bonded onto each other in such a manner that a temperature is elevated upto a softening point of the film substrate in a state where the substrate

20 and the thin film crystal semiconductor layer are brought in close contact with each other (in this case, the back-surface electrode is formed on the surface of the thin film crystal semiconductor layer in advance).

In the solar cell according to the present invention, 25 for the purpose of reducing the reflection loss of an incident light, the surface of the semiconductor layer can be subjected to a texture treatment. In case of

silicon, this treatment is conducted using hydrazine, NaOH, KOH or the like. The height of the piramid to be formed in the texture treatment is appropriately in a range of several to several tens μm .

5 Subsequently, an outline of steps of another producing method according to the present invention will be described referring to Figs. 5A to 5H.

10 First, as the first substrate 201 of crysalline, there is used, for example, a single-crystal semiconductor wafer. Impurities are introduced by thermal diffusion and ions implantation into the surface of the single-crystal semiconductor wafer or into the wafer during the production of the wafer so that a p^+ (or n^+) type layer is formed at least on the
15 wafer surface (Fig. 5A).

 Then, the wafer surface side where impurities are introduced is subjected to anodization in an HF solution to form the porous layer 202 (Fig. 5B).

20 Subsequently, the n^+ (or p^+)-type first single-crystal semiconductor layer 206 is allowed to epitaxially grow on the porous layer by the vapor phase growth method. Keeping the reducing atmosphere, the second single-crystal semiconductor layer 203 that functions as the active p^- (or n^-) type layer is allowed
25 to epitaxially grow on the single-crystal semiconductor layer 206 by the liquid phase growth method. Thereafter, if required, the third single-crystal

semiconductor layer 204 of the p⁺ (or n⁺) type layer is allowed to epitaxially grow (Fig. 5C).

Moreover, the second substrate 205 on which the back-surface electrode 209 has been formed in advance is bonded onto the p⁺ (or n⁺) type layer 204, or after the p⁺ (or n⁺) type layer 204 is formed, the back-surface electrode 209 is formed on the p⁺ (or n⁺) type layer 204, and thereafter the second substrate 205 is bonded onto the p⁺ (or n⁺) type layer 204 (Figs. 5D to 5E).

A force is exerted between the second substrate 205 and the first crystalline substrate 201 as bonded onto each other to then mechanically separate the porous layer 202, whereby the single-crystal semiconductor layers 204, 203 and 206 are transferred from the first crystalline substrate 201 to the second substrate 205 (Fig. 5F).

After transfer, the porous layer 202a remaining on the surface of the single-crystal semiconductor layer 206 is removed by etching, and then the transparent conductive layer 207 and the collecting electrode 208 are formed to provide a solar cell (Fig. 5G).

After the first crystalline substrate 201 as subjected to the separation step has the porous layer 202b remaining on its surface is removed and treated by etching, etc., it is again subjected to the initial step (Fig. 5A) as mentioned above (Fig. 5H).

As is apparent from the above description, the example shown in Figs. 5A to 5H is different from the example of Figs. 2A to 2I in that the thin film semiconductor layer is allowed to epitaxially grow on the porous layer by the vapor phase growth method, and thereafter the epitaxial growth is conducted by the liquid phase growth method as described with reference to Figs. 2A to 2I.

Subsequently, the vapor phase growth method for forming the thin film semiconductor layer will be described. As the vapor phase growth method, there are the thermal CVD method, the LPCVD method, the sputtering method, the plasma CVD method, the photo CVD method and so on. A source gas used for crystal growth is represented by silane or silane halide such as $\text{Si}_2\text{H}_2\text{Cl}_2$, SiCl_4 , SiHCl_3 , SiH_4 , Si_2H_6 , SiH_2F_2 or Si_2F_6 .

Also, as a carrier gas, or for the purpose of obtaining a reducing atmosphere that promotes crystal growth, hydrogen (H_2) is added together with the above-mentioned source gas. The mixture ratio of the source gas to hydrogen is properly set to be preferably 1:10 to 1:100 (introduction flow ratio) although it is appropriately determined according to the forming method, the kind of the source gas and also the forming conditions. The ratio is more preferably set to be 1:20 to 1:800.

In the case of forming the compound semiconductor

layer, the MOCVD method and the MBE method are used. As the source gas used for those crystal growth, for example, in the case of forming GaAs, $\text{Ga}(\text{CH}_3)_3$, AsH_3 , $\text{Al}(\text{CH}_3)_3$ or the like is used in the MOCVD method.

5 As a temperature at which growth is conducted, in the case of growing silicon by the thermal CVD method, it is appropriately set to about 800 to 1250°C, and it is desirable that the temperature is more preferably controlled to be 850 to 1200°C. Also, in the case of
10 growing GaAs by the MOCVD method, it is desirable that the temperature is controlled to 650 to 900°C. In the plasma CVD method, it is appropriately about 200 to 600°C, and more preferably 200 to 500°C.

 Similarly, a pressure is appropriately about 10^{-2}
15 to 760 Torr in methods other than the MBE method, and more preferably 10^{-1} to 760 Torr. In case of using the MBE method, the pressure as a back pressure is appropriately 10^{-5} Torr or less, and more preferably 10^{-6} Torr or less.

20 Then, the liquid phase growth method for forming a thicker crystal semiconductor layer on the crystal semiconductor layer that has grown by the vapor phase growth method will be described.

 The liquid phase growth can be basically conducted
25 by the above-mentioned method.

 However, when by the liquid phase method crystal is allowed to grow on the crystal semiconductor layer

that has grown by the vapor phase growth method, it is found that there is a case where some problems arise.

(Experiment 4)

5 A p-type silicon wafer having a porous layer formed in a surface region by a standard anodization was held in a hydrogen air flow at a surface temperature of $T_{surf} = 1050^{\circ}\text{C}$ for 30 minutes, and then the temperature went down to 900°C .

10 Then, n⁺-type crystal Si of $0.5\text{ }\mu\text{m}$ in thickness was deposited on the porous layer by the thermal CVD method by using hydrogen as a carrier gas, dichlorosilane (SiH_2Cl_2) as a source gas, and phosphine (PH_3) as dopant for n-type.

15 The silicon wafer extracted from the CVD apparatus was set in a liquid phase growing apparatus whose inside was made in a reducing atmosphere by a hydrogen air flow, and silicon was dissolved in a metal indium solvent of $T_m = 900^{\circ}\text{C}$ until the concentration became just a saturated state. Further, the wafer having the surface temperature $T_{surf} = 900^{\circ}\text{C}$ was immersed in a solution which was adjusted by addition of a slight amount of gallium (Ga) as a p-type dopant, and then gradually cooled at a cooling rate of $-1^{\circ}\text{C}/\text{min}$. As a result, a p⁻-type silicon layer of $25\text{ }\mu\text{m}$ in thickness
20 was deposited on the surface of the silicon wafer.
25 This was regarded as Sample 1.

For comparison, subsequent to formation of the

n⁺-type silicon layer, a p⁻-type silicon layer having the same thickness was deposited using the same CVD apparatus with diborane (B₂H₆) as a p-type doping gas. This was regarded as Sample 2.

5 Furthermore, for comparison, a p⁻-type silicon layer was deposited on the n⁺-type single-crystal wafer in the same manner as that of Sample 1. This was regarded as Sample 3.

10 As a result of observing the RHEED image of those samples, it could be recognized that epitaxial growth was made because a spot image was found in all the samples. In Samples 2 and 3, spots were clearer and streak lines and Kikuchi lines were observed. Thus, it was found that Samples had high quality crystal.

15 Further, the respective samples were immersed in an etching solution in which potassium dichromate was dissolved in an aqueous solution of hydrofluoric acid, and held for 5 minutes as it was for actuating defects (which is called "seco. etching"). As a

20 result, defects of about 10⁸/cm² were found in Sample 1 by observation through an optical microscope whereas only defects of about 10⁵/cm² were observed in Samples 2 and 3. That is, it has been found that when the film formed by the vapor phase growth method and the film

25 formed by the liquid phase growth method are stacked, an inherent problem occurs.

(Experiment 5)

The CVD apparatus and the liquid phase growing apparatus as used in Experiment 4 were modified in such a manner that they were connected to each other through a gate valve so that the sample could be transported without being exposed to atmosphere. First, an n'-type silicon layer was deposited on the p-type silicon wafer on which the same porous layer as formed in Experiment 4 was formed. Sequentially, while hydrogen was allowed to flow to the CVD apparatus side and the liquid phase growing apparatus side, the gate valve was opened, and the wafer was conveyed from the CVD apparatus side to the liquid phase growing apparatus side. Thereafter, a p'-type silicon layer was deposited by the liquid phase growth method as in Experiment 4. This was regarded as Sample 4.

Then, in order to recognize the effect of the modified apparatus, after crystal growth by the CVD method was completed and then the temperature of the sample was went down to the room temperature, the CVD apparatus side was opened to atmosphere. Thereafter, atmosphere was replaced by hydrogen, the sample was conveyed to the liquid phase growing apparatus side, and a p'-type silicon layer was deposited in the same manner as in Sample 1. This was regarded as Sample 5. The results of the RHEED image and the seco. etching clearly exhibited that Sample 4 was higher in crytallinity than Sample 5.

The present inventors interpret the results of Samples 4 and 5 as follows: That is, the surface of crystal whose growth is completed by the vapor phase growth has contamination such as chlorine. When this
5 contamination is exposed to atmosphere to break the reducing atmosphere, hydrolysis reaction occurs, and the oxidation of the surface is progressed, which adversely affects crystal growth. As a result, keeping the reducing atmosphere between the vapor phase growth
10 side and the liquid phase growth side can suppress the adverse influence of contamination.

(Experiment 6)

A series of samples were produced by using the same method as that of Sample 4 in Experiments 5,
15 provided that the surface temperature T_{surf} of the substrate was varied immediately before the substrate was immersed in the solution. All the samples exhibited excellent crystallinity. Then, an electrode of stacked magnesium and aluminum was deposited on the
20 surface of those samples. Magnesium was used for obtaining ohmic contact with the p⁻-type silicon. Since those samples had a junction of n⁺-type and p⁻-type, they exhibited the rectifying property as a diode. A ratio of a current value when +1 V is applied to p⁻-type
25 to a current value when -1 V is applied thereto is defined as a rectifying ratio, and the rectifying ratio of the respective Samples 6 to 10 are represented in

Table 3.

Table 3

	Tsurf	Rectifying Ratio
Sample 6	910°C	2×10^2
Sample 7	905°C	1×10^3
Sample 8	900°C	2×10^4
Sample 9	895°C	5×10^5
Sample 10	890°C	1×10^6

As shown in Table 3, higher rectifying ratio is obtained when Tsurf is lower than the solution temperature ($T_m = 900^\circ\text{C}$). When Tsurf is higher, etch-back occurs immediately after the substrate is immersed in the solution, and n-type dopant starts to be immersed in the solution. When deposition is again conducted before the n-type dopant is not sufficiently diffused, n-type dopant is considered to be mixed into the active layer which should be naturally of p⁻-type, thereby adversely affecting the junction characteristic.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic cross-sectional view showing an example of the structure of a solar cell;

Figs. 2A, 2B, 2C, 2D, 2E, 2F, 2G, 2H and 2I are schematic views for explaining an example of steps of a method of forming a semiconductor member or a

semiconductor device;

Fig. 3 is a graph showing a relationship between the concentration and temperature of a solute;

Fig. 4 is a schematic cross-sectional structural view for explaining an example of a producing apparatus;

Figs. 5A, 5B, 5C, 5D, 5E, 5F, 5G and 5H are schematic views for explaining another example of steps of a method of forming a semiconductor member or a semiconductor device;

Fig. 6 is a schematic cross-sectional structural view for explaining another example of a producing apparatus;

Fig. 7 is a schematic cross-sectional structural view for explaining another example of a producing apparatus;

Figs. 8A, 8B, 8C, 8D, 8E, 8F, 8G and 8H are schematic processing views for explaining another example of steps of a method of forming a semiconductor member or a semiconductor device;

Fig. 9 is a schematic cross-sectional view showing another example of the structure of a solar cell;

Figs. 10A, 10B, 10C, 10D, 10E, 10F, 10G, 10H, 10I, 10J, 10K, 10L and 10M are schematic processing views for explaining another example of steps of a method of forming a semiconductor member or a semiconductor device;

Figs. 11A, 11B, 11C, 11D, 11E, 11F, 11G, 11H, 11I and 11J are schematic views for explaining an example of steps of a method of forming a semiconductor member or a semiconductor device; and

5 Figs. 12A, 12B, 12C, 12D, 12E, 12F, 12G, 12H, 12I, 12J, 12K, 12L, and 12M are schematic views for explaining another example of steps of a method of forming a semiconductor member or a semiconductor device.

10

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Examples of the producing method according to the present invention will be given below in more detail with reference to the accompanying drawings. The
15 present invention is described in the above, and the present invention is not limited to the following Examples.

(Example 1)

20 This Example exhibits a method of forming a solar cell by transferring a single-crystal silicon layer to a polyimide film by the steps shown in Figs. 2A to 2I.

Boron (B) was thermally diffused at a temperature of 1200°C into the surface of single-crystal silicon wafer 201 of 500 μm in thickness by using BCl_3 as a heat
25 diffusion source to form a p^+ type layer and obtain a diffusion layer of about 3 μm (Fig. 2A). Then, anodization was conducted in an HF solution under the

condition shown in Table 4 to form a porous silicon layer 202 on the wafer (Fig. 2B).

Table 4

Anodization Solution	HF: H ₂ O:C ₂ H ₅ OH = 1:1:1
Current Density	5 mA/cm ² → 30 mA/cm ²
Anodization Time	2.5 min → (30 sec) → 0 sec

Then, by using a method of gradually cooling, liquid phase epitaxial growth of silicon was conducted. First, metal indium (In) was melted within the carbon boat in a hydrogen air flow at 900°C. A polycrystal wafer was dissolved while stirring the solution therein until it became saturated. Then, the solution temperature slowly went down to 894°C to provide a crystal growth solution. Thereafter, the atmospheric temperature was adjusted so that the temperature of the single-crystal silicon wafer on which the porous layer 202 was formed in the hydrogen air flow was set to 1030°C, and then annealed for 1 hour. Thereafter, the temperature was lowered, and waiting was made until it became identical with the temperature of the solution. In this state, the wafer having the porous layer formed on the surface was immersed in the solution, and was gradually cooled at a cooling rate of -1.0°C/min. A non-doped thin film silicon layer 203 of 20 μm in thickness was deposited on the porous layer 202, and was then lifted up from the solution (Fig. 2C).

Subsequently, metal indium (In) was melted at 900°C within a carbon boat separately provided and was saturated with Si. Further, gallium (Ga) containing Si of 0.1 atomic% was melted to provide a crystal growth solution. Sequentially, the wafer on which the non-doped thin-film silicon layer was formed was immersed in the solution to deposit the p⁺ type thin film silicon layer 204 having thickness of 1 μm on the thin film silicon, and then lifted up from the solution (Fig. 2D).

The copper paste 209 was coated in thickness of 20 μm on one surface of the polyimide film 205 having a thickness of 50 μm by screen printing, and that surface was brought in close contact with and bonded to the surface of the above-mentioned p⁺ type thin film silicon layer 204 of the wafer. In this state, it was put into an oven so that the copper paste was sintered under the condition of 300°C and 20 minutes, and the polyimide film and the wafer were bonded onto each other (Fig. 2E). In the polyimide film and the wafer as bonded onto each other, another surface of the wafer which was not bonded was fixed by a vacuum chuck (not shown in the drawing), and a force was exerted from one end of the polyimide film 205 to conduct peeling in such a manner that the silicon layers 203 and 204 were separated from the wafer 201 and then transferred onto the polyimide film 205 (Fig. 2F).

The remainder (porous layer 202a) of the porous layer 202 which remained on the thin film silicon layer 203 after separation from the wafer 201 was selectively etched while being stirred with a mixture solution consisting of hydrofluoric acid, hydrogen peroxide water and pure water. The thin film silicon layer 203 remained without being etched, and only the remainder of the porous layer 202 was completely removed. In the non-porous silicon single-crystal, the etching rate by using the above-mentioned etching solution is very low, and the selective ratio of the etching rate of the porous layer to that of the non-porous layer reaches 10^5 or more so that the etching amount of the non-porous layer (about several tens Å) can be ignored in practical use. As a result of observing the section of the layer by a transparent electron microscope, it has been recognized that excellent crystallinity is maintained without introducing new crystal defects into the thin film silicon layer 203. After the surface of the thin film silicon layer 203 on the polyimide film 205 as obtained was etched with an etching solution of hydrofluoric acid/nitric acid for cleaning, the microcrystal silicon (hereinafter referred to as "µc-Si") layer 206 of n-type was deposited in thickness of 200 Å on the thin film silicon layer 203 by a plasma CVD apparatus available in the market under the conditions shown in Table 5. In this situation, the

dark conductivity of the $\mu\text{c-Si}$ layer was 5 S/cm, where S (siemens) is the inverse number of ohm (Ω).

Table 5

5	Gas Flow Amount Ratio	$\text{SiH}_4/\text{H}_2 = 1 \text{ cc}/20 \text{ cc}$ $\text{PH}_3/\text{SiH}_4 = 2.0 \times 10^{-3}$
	Substrate Temperature	250°C
	Pressure	0.5 Torr
	Discharge Power	20 W

10 Finally, an ITO transparent conductive film (82 nm thick) and a collecting electrode (Ti/Pd/Ag (400 nm/200 nm/1 μm thick)) were formed on the $\mu\text{c-Si}$ layer by the EB (electron beam) vapor deposition to provide a solar cell (Fig. 2H).

15 As a result of measuring the I-V characteristic of the solar cell obtained by using single-crystal silicon on a polyimide thin film under illumination of AM 1.5 (100 mW/cm^2) light, the conversion efficiency of 14.6% was obtained.

20 Also, the porous layer that remains on the silicon wafer 201 separated was removed by etching in the same manner as described above to produce a smooth surface (Fig. 2I). By using the regenerated wafer thus obtained, the above-mentioned steps were repeated to
25 obtain a plurality of thin film single-crystal solar cells having a semiconductor layer with high quality.

(Example 2)

In this example, a solar cell having the same structure as that of Example 1 was fabricated. In the same manner as that of Example 1, the porous silicon layer 202 was formed on the surface of the single-crystal silicon wafer 201.

Then, by using a method which is called "temperature difference method", liquid phase epitaxial growth of silicon was conducted. In this example, the apparatus as shown in Fig. 6 was used which was different in internal structure of the liquid phase growth vessel from the apparatus as shown in Fig. 4. In other words, as shown in Fig. 6, an Si wafer (polycrystal silicon wafer) 418 is stuck onto the right-sided inner wall of the carbon board 414, and also a balance of the heaters 413 and 417 is changed and adjusted in such a manner that a temperature of the right side of the carbon board becomes higher. Therefore, silicon starts to be dissolved under the condition where the solution is non-saturated, and dissolved silicon is diffused leftward. At this side, because the temperature is low so that the solution is supersaturated, silicon is deposited.

First, metal indium (In) was melted at 900°C within the carbon boat in a hydrogen air flow. Then, a polycrystal silicon wafer 419 for dissolution was immersed in the melted indium and stuck onto a part of the inner wall of the boat. Then, the wafer 419 was

dissolved and saturated while being stirred.

Subsequently, the temperature of the solution was

slowly lowered to 890°C to provide a crystal growth

solution. Thereafter, after annealing in the hydrogen

5 air flow, the atmospheric temperature was adjusted, and

waiting was made until the temperature of the single-

crystal silicon wafer 201 on which the porous layer 202

was formed became identical with the temperature of the

10 solution. In this state, the wafer 201 on a surface of

which the porous layer was formed was immersed in the

solution, and the temperature of the wall surface of

the boat to which the Si wafer was stuck was set to

910°C while the peripheral temperature of the single-

crystal silicon wafer 201 was adjusted so as not to be

15 changed. Thereafter, in a manner different from

Example 1, the wafer was left without any change in the

temperature of the solution, etc., and the non-doped

thin film silicon layer 203 was deposited in thickness

of 20 μm on the porous layer 202 and then lifted up

20 from the solution. In the temperature difference

method, since the solution close to the polycrystal

silicon wafer for dissolution is non-saturated and

silicon continues to be dissolved from the surface of

the wafer in a stationary manner, there is no necessity

25 of cooling the entire solution. Subsequently, metal

indium (In) was melted at 900°C within another carbon

boat separately provided and saturated with Si.

Further, gallium (Ga) containing Si of 0.1 atomic% was melted, and then the temperature was lowered to 890°C to provide a crystal growth solution. Sequentially, the wafer on which the non-doped thin-film silicon layer was formed was immersed in the solution to deposit the p⁺ type thin film silicon layer 204 having the thickness of 1 μm on the thin film silicon, and then lifted up from the solution. In this case, because the growth time was short, the thin film silicon layer could be nearly deposited in a stationary manner even without gradually cooling or using the silicon wafer for dissolution.

In the subsequent step, by the same manner as that in Example 1, the thin film single-crystal silicon solar cell was formed on the polyimide film. As a result of measuring the I-V characteristic of the solar cell obtained by using the single-crystal silicon on the polyimide thin film under illumination of AM 1.5 (100 mW/cm²) light, the conversion efficiency of 15.4% was obtained.

Also, the porous layer that remained on the silicon wafer as separated was removed by etching in the same manner as described above to produce a smooth surface (Fig. 2I). Using the regenerated wafer thus obtained, the above-mentioned steps were repeated to obtain a plurality of thin film single-crystal solar cells having a semiconductor layer with high quality.

(Example 3)

In this example, a solar cell having the same structure as that of Example 1 was fabricated. In the same manner as that of Example 1, the porous silicon
5 layer 202 was formed on the surface of the single-crystal silicon wafer 201.

Then, by a method which is called "constant-temperature method" as disclosed in Japanese Patent Application Laid-Open No. 6-191987 by the present
10 inventors, liquid phase epitaxial growth of silicon was conducted. In this example, the apparatus as shown in Fig. 7 was used which was different in the internal structure of the liquid phase growth vessel from the apparatus shown in Fig. 4. In other words, the
15 substrate and polycrystal silicon wafer 418 are disposed opposite to each other. Because silicon dissolved out from the polycrystal silicon causes convection due to change of the density in the solution so that silicon is transported to the substrate side
20 and deposited thereon. In order to effectively generate this convection, a distance between the substrate and polycrystal silicon needs to be kept long.

First, metal indium (In) was melted at 900°C within the carbon boat in a hydrogen air flow. Then, a
25 polycrystal silicon wafer for dissolution was immersed in the melted indium and stuck onto the bottom of the boat. Then, the wafer was dissolved and saturated.

Subsequently, the temperature of the solution was slowly lowered to 894°C to provide a crystal growth solution. Thereafter, waiting was made until the temperature of the single-crystal silicon wafer 201 on which the annealed porous layer 202 was formed became equal to the temperature of the solution. In this state, the wafer 201 on a surface of which the porous layer was formed was immersed in the solution, and the surface of the porous layer 202 was opposed to the polycrystal silicon wafer for dissolution at an interval of 2 cm. Thereafter, in manners different from Example 1, without any change in the temperature of the solution, etc., and different from Example 2, without generating the temperature difference in the solution, the solution was left, and the non-doped thin film silicon layer 203 was deposited in thickness of 20 μm on the porous layer 202 and then lifted up from the solution. In the constant-temperature method, since the solution close to the polycrystal silicon wafer for dissolution is lowered in density by dissolution of Si in the solution, Si is carried away toward the surface of the porous silicon layer 202 due to convection. As a result, silicon continues to be dissolved from the surface of the wafer in a stationary manner and therefore there is no necessity of cooling the entire solution. Thereafter, by the same manner as that of Example 1, the thin film single-crystal silicon solar

cell was formed on the polyimide film. As a result of measuring the I-V characteristic of the obtained polyimide thin film/single-crystal silicon using solar cell under illumination of AM 1.5 (100 mW/cm^2) light, the conversion efficiency of 16.2% was obtained under the conditions that a cell area was 6 cm^2 , an open voltage was 0.6 V, a short-circuit photo current was 35 mA/cm^2 , and a curve factor was 0.79.

Also, the porous layer that remains on the silicon wafer as separated was removed by etching in the same manner as described above to produce a smooth surface (Fig. 2I). Using the regenerated wafer thus obtained, the above-mentioned steps were repeated to obtain a plurality of thin film single-crystal solar cells having a semiconductor layer with high quality.

(Example 4)

In this example, a thin film single-crystal solar cell was fabricated in the same manner as that of Example 1 except that the surface temperature T_{surf} of the single-crystal silicon wafer 201 to be immersed in the solution of $T_{\text{sat}} = T_m = 890^\circ\text{C}$. Similarly, as a result of measuring the I-V characteristic of the obtained polyimide thin film/single-crystal silicon using solar cell under illumination of AM 1.5 (100 mW/cm^2) light, the conversion efficiency of 16.2% was obtained.

(Example 5)

The steps in this example are common to the steps

of Example 1 until the non-doped thin film silicon layer 203 is deposited. The sample lifted up from the solution was heated up to 1,200°C in a hydrogen air flow, and left for 30 minutes. Then, the temperature was again adjusted to 900°C. By this heat treatment, boron (B) in the p-type porous layer 202 was thermally diffused into the non-doped thin film silicon layer 203 to produce the p⁺ type thin film silicon layer 206. Subsequently, metal indium (In) was melted at 900°C within another carbon boat separately provided and saturated with Si. Further, antimony (Sb) containing Si of 0.1 atomic% was melted to provide a crystal growth solution. Sequentially, the wafer on which the non-doped thin-film silicon layer 203 was formed was immersed in the solution to deposit the n⁺ type thin film silicon layer 204 in thickness of 1 μm on the thin film silicon, and then lifted up from the solution. Thereafter, the thin film single-crystal solar cell inverse in the order of the doped layers to that of Example 1 was fabricated in the same manner as that of Example 1 except that the step of depositing the n-type microcrystal silicon (μc-Si) layer 206 by the plasma CVD apparatus was omitted. Similarly, as a result of measuring the I-V characteristic of the obtained polyimide thin film/single-crystal silicon using solar cell under illumination of AM 1.5 (100 mW/cm²) light, the conversion efficiency of 15.7% was obtained.

(Example 6)

In this example, a solar cell having the same structure as that of Example 1 was fabricated using the steps shown in Figs. 8A to 8H. In this example, first, the same steps as that of Example 1 were conducted except that an n⁺-type thin film silicon layer is formed on the porous layer 202 as the n⁺ (or p⁺) type layer 206 by the epitaxial method.

That is, in this example, as shown in Fig. 8B, by the same method as that in Example 1, the porous silicon layer 202 was formed in the surface region of single-crystal silicon wafer 201. Then, metal indium (In) was melted at 800°C within a carbon boat in a hydrogen air flow. The polycrystal silicon wafer was dissolved while the solution was stirred, and then saturated. Further, antimony (Sb) containing Si of 0.2 atomic% was melted to provide a crystal growth solution. Then, the temperature of the solution was slowly lowered to 794°C to provide a crystal growth solution. Thereafter, the atmospheric temperature was adjusted, and waiting was made until the temperature of the single-crystal silicon wafer 201 on which the annealed porous layer 202 was formed became equal to the temperature of the solution. In this state, the wafer on a surface of which the porous layer was formed was immersed in the solution, and gradually cooled at a cooling rate of -1.0°C/min to deposit the n⁺ type thin

film silicon layer 206 having a thickness of 0.5 μm on the porous layer 202 and lifted up from the solution. Then, in the same manner as that in Example 1, the non-doped thin film silicon layer 203 having a thickness of 20 μm and the p^+ type thin film silicon layer 204 having a thickness of 1 μm were deposited. Thereafter, the thin film single-crystal solar cell having the same order of the doped layers as that of Example 1 was fabricated in the same manner as that of Example 1 except that the step of depositing the n^+ -type microcrystal silicon ($\mu\text{c-Si}$) layer 206 by the plasma CVD apparatus was omitted. Similarly, as a result of measuring the I-V characteristic of the obtained polyimide thin film/single-crystal silicon solar cell under illumination of AM 1.5 (100 mW/cm^2) light, the conversion efficiency of 16.4% was obtained.

(Example 7)

In this example, the p-type layer formed by the liquid phase growth method instead of the heat diffusion was anodized. First, metal indium (In) was melted within the carbon boat in a hydrogen air flow at 900°C. Then, a polycrystal silicon wafer was dissolved and saturated while the solution was stirred. Moreover, gallium (Ga) containing Si of 0.1 atomic% was melted to provide a crystal growth solution. In this state, the single-crystal silicon wafer 201 having a thickness of 500 μm and the same temperature was

immersed in the solution, and gradually cooled at a cooling rate of $-1.0^{\circ}\text{C}/\text{min}$, to thereby form a p-type semiconductor layer of $3\text{ }\mu\text{m}$ in thickness. In the subsequent steps, the thin film single-crystal silicon solar cell having the same structure was obtained in the same procedure as that of Example 1.

Also, the porous layer that remained on the silicon wafer 201 as separated was removed by etching in the same manner as described above to produce a smooth surface (Fig. 2I). Thereafter, the p-type semiconductor layer of $3\text{ }\mu\text{m}$ in thickness was again formed by the above liquid phase growth method, and the thin film single-crystal solar cell having the same structure was obtained in the same procedure as that of Example 1. Thereafter, using the same single-crystal silicon wafer 201 in the same manner, there was obtained a large number of thin film single-crystal solar cells having a semiconductor layer with high quality. By conducting these steps, not only the expensive single-crystal silicon wafer 201 can be effectively utilized, but also the step of thermally diffusing B is not required.

(Example 8)

In this example, the thin film polycrystal solar cell was obtained by using the thin film polycrystal formed on the polyimide film in the same manner as that of Example 1 except that the polycrystal silicon wafer

of 1,000 μm in thickness and mainly about 0.3 to 3 cm in the diameter of grains was used as the first substrate instead of the single-crystal silicon wafer. In the solar cell as obtained in this manner, it is
5 presumed that crystal orientation of the polycrystal silicon wafer is transferred up to the non-doped layer within the respective crystal grain regions of the polycrystal silicon wafer as used, and epitaxial growth occurs locally. As a result of measuring the I-V
10 characteristic of the obtained thin film polycrystal silicon solar cell thus obtained under illumination of AM 1.5 (100 mW/cm^2) light, the conversion efficiency of 13.5% was obtained.

Also, the porous layer that remained on the
15 silicon wafer 201 as separated was removed by etching in the same manner as described above to produce a smooth surface (Fig. 2I). By using the economical regenerated wafer as thus obtained, the above-mentioned steps were repeated to obtain a plurality of thin film
20 polycrystal solar cells having a semiconductor layer high in quality.

(Example 9)

In this example, the polycrystal silicon substrate produced in such a manner that ingot upgraded from the
25 inexpensive metal-graded silicon 98.5% in nominal purity by the CZ (Czochralski) method was sliced into pieces 1 mm in thickness, and the surfaces of a wafer

was mirror-ground and the wafer was used the first substrate 201. The metal-graded silicon is inexpensive coarse silicon which is used also as a raw material of aluminum alloy or the like. Although this silicon is very inexpensive in comparison with normal silicon for semiconductor, there is no case where it is used for electric devices as it is because it contains impurities with high concentration. As a result of analyzing the elements near the surface the metal-graded silicon substrate as produced, the concentration of impurities was slightly more than 0.01% (the purity of Si was slightly less than 99.99) in total, as shown in Table 6. Also, the diameter of the crystal grains of the metal-graded silicon substrate was several mm to several cm (Fig. 2A).

Table 6

Impurity	Concentration
Ca	42 ppm
B	38 ppm
Al	22 ppm
Ni	< 5 ppm
Fe	10 ppm
Cr	0.6 ppm
Mn	< 0.2 ppm
Ti	< 1 ppm

On this wafer, the non-doped layer of 1 μm in thickness and the p-type layer of 3 μm in thickness

were formed in this order by the liquid phase growth method as described in Example 7 and then this p-type layer was anodized. As shown here, there are many cases where the metal-graded silicon is of p-type, but because the degree of doping is unstable, the reproducibility of the anodization is liable to be deteriorated. The p-type layer controlled by the liquid phase growth method is formed and subjected to anodization, thereby being capable of improving the reproducibility of the anodization. Further, by interposing a non-doped layer between the polycrystal silicon and the p-type layer formed by the liquid phase growth method, the controllability of the depth of the anodization is improved. The subsequent steps were conducted in the same procedure as that of Example 1 to obtain the thin film polycrystal silicon solar cell having the same structure.

Also, the porous layer that remained on the silicon wafer 201 as separated was removed by etching in the same manner as described above to produce a smooth surface (Fig. 2I). Thereafter, the non-doped layer of 1 μm in thickness and the p-type layer of 3 μm in thickness were again formed by the above liquid phase growth method to obtain the thin film polycrystal solar cell having the same structure in the same procedure as that of Example 1. Thereafter, the same procedure was repeated, using the same metal-graded

polycrystal silicon wafer to obtain a still larger number of thin film polycrystal solar cells having a semiconductor layer with high quality. By conducting these steps not only the low-graded polycrystal silicon wafer could be utilized, but also the step of thermally diffusing B was not required.

(Example 10)

In this example, there is shown a method in which the compound semiconductor layer having the structure as shown in Fig. 9 is transferred to acrylic resin to form a super-high efficient tandem type solar cell.

In Fig. 9, reference numeral 901 denotes a substrate; 902, a porous layer; 903, an n^+ type layer; 904, an n^+ type layer; 905, an n type layer; 906, a p type layer; 907, a p^+ type layer; 908, a p type layer; 909, an n^+ type layer; 910, an n type layer; 911, an n^+ type layer; 912, an n type layer; and 913, a p type layer. Therefore, the respective conductive type semiconductor layers are formed on the porous layer 902 in the order of $n^+/n^+/n/p/p^+/p/n^+/n/n^+/n/p$.

In this example, the compound semiconductor is used, and the composition of the respective layers are stated below.

The n^+ type layer 903 is n^+ type GaAs; the n^+ type layer 904 is n^+ type $Al_xGa_{1-x}As$; the n type layer 905 is n type $Al_{0.37}Ga_{0.63}As$; the p type layer 906 is p type $Al_{0.37}Ga_{0.63}As$; the p^+ type layer 907 is

p⁺ type Al_{0.37}Ga_{0.63}As; the p type layer 908 is p type Al_{0.37}Ga_{0.63}As; the n⁺ type layer 909 is n⁺ type Al_xGa_{1-x}As; the n type layer 410 is n type Al_{0.37}Ga_{0.63}As; the n⁺ type layer 411 is n⁺ type Al_{0.9}Ga_{0.1}As; the n type layer 412 is n type GaAs; and the p type layer 413 is p type GaAs.

Then, a specific producing example will be described.

First, B (boron) was thermally diffused into the surface of single-crystal silicon wafer of 500 μm in thickness as the substrate 901 by using BCl₃ as a heat diffusion source at a temperature of 1,200°C to form a p⁺ type layer and obtain a diffusion layer of about 3 μm. Then, anodization was conducted in an HF solution under the condition shown in Table 7 to form on the wafer a porous silicon layer as the porous layer 902.

Table 7

Anodization Solution	HF: H ₂ O:C ₂ H ₅ OH = 1:1:1
Current Density	1 mA/cm ² → 5 mA/cm ² → 40 mA/cm ²
Anodization Time	2 min → 2.5 min → (30 sec) → 0 sec

Then, by the gradually cooling method, liquid phase hetero-epitaxial growth of silicon was conducted. First, metal gallium (Ga) was melted within the carbon boat in a hydrogen air flow at 810°C. Arsenic (As) was dissolved in the melted indium until it became saturated. On the other hand, after the porous layer

902 was annealed at 1,050°C in a hydrogen atmosphere for 7 minutes, the temperature was lowered to 800°C. Thereafter, the solution temperature was adjusted to 800°C, and the single-crystal silicon wafer on which the porous silicon layer 902 was formed was immersed in the solution, and the solution temperature was slowly lowered at a rate of -0.1°C/min to allow the n⁺ type GaAs layer 903 to grow. Then, aluminum (Al) was brought in contact with the gallium solution and gradually dissolved in the solution to continue the crystal growth, thereby growing a transition layer 904 (mentioned as Al_xGa_{1-x}As) of n⁺ type in which the concentration of Al was gradually varied. When attaining at x = 0.37, the contact of Al with gallium solution was suspended, and while the concentration of Al was kept constant, the n type Al_{0.37}Ga_{0.63}As layer was allowed to grow. Then, the substrate on which up to the n type Al_{0.37}Ga_{0.63}As layer was formed was immersed into another Ga solution of 800°C containing Al and As with p-type dopant which was separately prepared. Then, the solution was cooled at -0.1°C/min to grow the p-type Al_{0.37}Ga_{0.63}As. Further, the amount of dopant was increased to grow the p⁺-type Al_{0.37}Ga_{0.63}As layer. By the same procedure as mentioned above, the p-type Al_{0.37}Ga_{0.63}As layer, the n⁺-type Al_xGa_{x-1}As layer, the n-type Al_{0.37}Ga_{0.63}As layer, the n⁺-type Al_{0.9}Ga_{0.1}As layer, the n-type GaAs layer, and the p-type GaAs layer were

allowed to grow.

After Pd/Au was formed on the p-type GaAs layer which was the outermost layer formed by the EB vapor deposition, a copper paste was coated in thickness of 10 to 30 μm on one surface of an acrylic plate having a thickness of 1 μm by screen printing, and the coated surface was brought in close contact with and bonded to the above-mentioned wafer p⁺ type GaAs layer side. In this state, it was put into an oven so that the copper paste was sintered under the condition of 300°C and 20 minutes, and the acrylic resin plate and the wafer were bonded onto each other. In the acrylic resin plate and the wafer as bonded onto each other, another non-bonded surface of the wafer and another non-bonded surface of the acrylic resin plate were fixed by a vacuum chuck (not shown in the drawing), respectively, and a tensile was uniformly exerted on those chucks perpendicularly to the bonded surfaces so that the porous layer 902 was destroyed to separate the growth layer from the wafer and transferred onto the acrylic resin plate. The porous layer which remained on the n⁺ type GaAs layer which was separated from the silicon wafer was selectively etched with a mixture solution of ethylene diamine, pyrocatechol and pure water at 110°C. The n⁺ type GaAs layer remained without being etched, and only the porous layer was completely removed. The etching rate of single-crystal GaAs by using the

above-mentioned etching solution is very low so that the reduction of the thickness can be ignored in practical use. As a result of observing the section of the layer by a transparent electro-microscope, it has
5 been recognized that excellent crystallinity is maintained such that a new crystal defect is not introduced in the growth layer.

Then, the n^+ type GaAs layer which was the outermost surface layer was allowed to remain in the
10 shape of a grid by etching other portions than the grid so that the n^+ type $Al_xGa_{1-x}As$ layer was exposed, and then the surface electrode (Au/Ge/Ni/Au) was formed only on the grid-shaped n^+ type GaAs layer by the EB vapor deposition and photolithgraphy. Thereafter,
15 TiO_2/MgO was deposited as a reflection preventing layer by the plasma CVD method to provide a solar cell.

As a result of measuring the I-V characteristic of the obtained thin film compound semiconductor silicon solar cell using the acrylic resin plate under
20 illumination of AM 1.5 (100 mW/cm^2) light, the conversion efficiency of 23.8% was obtained.

Also, the porous layer that remained on the silicon wafer as separated was removed by etching in the same manner as described Examples 1 and 2 to
25 produce a smooth surface. By using the regenerated wafer as thus obtained, the above-mentioned steps were repeated to obtain a plurality of thin film compound

semiconductor solar cells having a semiconductor layer with high quality.

(Example 11)

5 In this example, an example of producing a stagger type field effect transistor using the single-crystal silicon will be described with reference to the steps shown in Figs. 10A to 10M.

As a substrate, the single-crystal silicon wafer 601 having thickness of 500 μm was prepared (Fig. 10A).
10 Then, B was thermally diffused on the surface of the single-crystal silicon wafer 601 with BCl_3 as the thermal diffusion source at a temperature of $1,200^\circ\text{C}$ to form a p^+ type layer, thus obtaining a diffusion layer of about 3 μm . Subsequently, in the same manner as
15 that of Example 1, the porous layer 602 was obtained (Fig. 10B). Then, the liquid phase epitaxial growth of silicon was conducted by the gradually cooling method. That is, first, a saturated solution of 900°C was prepared within the carbon board in a hydrogen air
20 flow, and arsenic (As) was dissolved as the n-type dopant, and then the temperature of the solution was slowly lowered to 894°C to provide a crystal growth solution. Then, the atmospheric temperature was adjusted so that the temperature of the single-crystal
25 silicon wafer 601 on which the porous layer 602 was formed in the hydrogen air flow was set to $1,030^\circ\text{C}$, and then annealed for 1 hour. Thereafter, the temperature

was lowered, and waiting was made until it became equal to the temperature of the solution. In this state, the wafer on a surface of which the porous layer was formed was immersed in the solution so that the thin film silicon layer 603 of 0.1 μm in thickness was deposited on the porous layer 602 (Fig. 10C). Subsequently, a saturated solution of 900°C was prepared within another carbon boat, and the temperature of the solution in the another carbon boat was slowly lowered to 894°C. The wafer on which the n^+ type thin-film silicon layer 603 was formed was immersed in the solution to deposit the p^- type thin film silicon layer 604 having thickness of 0.3 μm thereon, and then lifted up from the solution (Fig. 10D). Then, the surface side of the p^- type thin film silicon layer 604 was oxidized to 0.1 μm in depth by the heat treatment in a steam to provide a gate insulated film (Fig. 10E). On the film, an aluminum film was deposited by the sputtering method, and a gate electrode/gate wiring 606 were formed by the photolithography process (Fig. 10F). On the film, the glass substrate 608 was stuck through the SiO_2 film 607 by the sol/gel method (Fig. 10G). Thereafter, the wafer 601 was separated at the portion of the porous layer 602 (Fig. 10H), and after the remainder of the porous layer 602 was removed (Fig. 10I), the n^+ type thin film silicon layer 603 was patterned as indicated by reference numerals 603' and 603" by the

photolithography process (Fig. 10J). Moreover on the film, a silicon nitride film 609 was deposited, and contact holes for source/drain electrodes were patterned by the photolithography process (Fig. 10K).

5 Further, an aluminum layer was deposited and patterned by the photolithography process, to thereby form the drain electrode/drain wiring 610' and the source electrode/source wiring 610" (Fig. 10L).

10 Since the transistor thus produced had thin p⁻ type layer of single-crystal, it obtained very high on/off ratio of the drain current by the on/off of the gate voltage, and also obtained large drain current. Therefore, even when the area of the transistor is small, a large drive performance is provided. Also, 15 since it is of the stagger type although single-crystal is used, the free degree of the drain/gate wiring is as large as that of the transistor using amorphous silicon, and when the transistor is used for the matrix driving of liquid crystal, the high contrast, the high- 20 speed operation and the high opening degree can be readily realized. Similarly, the remaining porous layer 602 is removed from the single-crystal silicon wafer 601 as separated (Fig. 10M), and it is reused as occasion demands.

25 (Example 12)

In this example, an example of fabricating an LED of GaAlAs type will be described by using the steps

shown in Figs. 11A to 11J. First, a GaAlAs wafer 701 was prepared (Fig. 11A). Then, the single-crystal p-type GaAs wafer 701 having a thickness of 800 μm was anodized under the conditions shown in Table 8 to form a porous layer 702, taking "Report by P. Schmuki, et al. (P. Schmuki, J. Fraser, C.M. Vitus, M.J.. Graham, H.S. Issacs J. Electrochem, Soc. 143 (1996) pp. 3316)" into account (Fig. 11B).

Table 8

Anodization Solution	HCl: H_2SO_4 : $\text{NH}_4\text{H}_2\text{PO}_4$ = 1:1:3
Applied Voltage	300 V \rightarrow 1,000 mA/ cm^2
Anodization Time	1 min \rightarrow 5 sec

Then, liquid phase hetero-epitaxial growth of compound semiconductor was conducted. First, metal gallium (Ga) was melted within the carbon boat in a hydrogen air flow at 810°C. Arsenic (As) was dissolved in the melted indium until it became saturated. Thereafter, the solution temperature was adjusted to 800°C, and while the single-crystal silicon wafer 701 on which the porous silicon layer 702 was formed was immersed in the solution, aluminum (Al) was brought in contact with the solution and gradually dissolved in the solution to continue the crystal growth, whereby the transition layer ($\text{Al}_x\text{Ga}_{1-x}\text{As}$) where the concentration of Al was gradually varied was allowed to grow (Fig. 11C). The growth of the transition layer 703 was

conducted with being immersed in the solution at the surface temperature of 800°C. The gradually cooling condition was set to -0.1°C/min. When attaining at $x = 0.37$, the contact of Al with gallium solution was

5 suspended, and while the concentration of Al was kept constant, the $\text{Al}_{0.37}\text{Ga}_{0.63}\text{As}$ layer 704 was allowed to grow (Fig. 11D). Then, by using another solution as separately prepared, a light emitting layer $\text{Al}_{0.5}\text{Ga}_{0.5}\text{As}$ layer 705 was grown (Fig. 11E). Again, as the barrier

10 layer, an $\text{Al}_{0.37}\text{Ga}_{0.63}\text{As}$ layer 706 was grown (Fig. 11F). Subsequently, a glass 709 coated with an SnO_2 transparent conductive layer 708 was bonded to sol-gel film 708 of In_2O_3 (Fig. 11G), and then wafer 701 was separated (Fig. 11H). Moreover, a glass 711 was bonded

15 to the separated glass 709 side by a copper paste layer 710, and a lead line 712 was drawn out from the SnO_2 transparent conductive layer 708 and the copper paste layer 710 (Fig. 11I). In this way, the side surfaces were sealed with a resin 713 (Fig. 11J). In this way,

20 high-luminant face light emitting red color LED could be obtained. In this way, in particular, an emitted light is effectively reflected on the surface of the copper paste layer 710, and because the SnO_2 transparent conductive layer 708 and the sol-gel film 707 of In_2O_3

25 reduce a reflection loss due to a large difference in the refractive ratio between the glass 711 and the $\text{Al}_{0.37}\text{Ga}_{0.63}\text{As}$ layer 706, luminance becomes

high.

(Example 13)

This example shows an example of a method of forming a solar cell by transferring a single-crystal silicon layer onto a polyimide film by the wteps shown in Figs. 5A to 5H, using an apparatus shown in Fig. 4.

First, as a substrate 201, the single-crystal silicon wafer having thickness of 500 μm was prepared (Fig. 5A). Then, B was thermally diffused on the surface of the single-crystal silicon wafer with Bcl_3 as the thermal diffusion source at a temperature of 1,200°C to from a P⁺ type layer, thus obtaining a diffusion layer of about 3 μm in thickness.

Then, anodization was conducted under the condition shown in Table 9 in an HF solution to form a porous silicon layer on the wafer as a porous layer 202 (Fig. 5B).

Table 9

Anodization Solution	$\text{HF}:\text{H}_2\text{O}:\text{C}_2\text{H}_5\text{OH} = 1:1:1$
Current Density	$5 \text{ mA/cm}^2 \rightarrow 30 \text{ mA/cm}^2$
Anodization Time	$2.5 \text{ min} \rightarrow (30 \text{ sec}) \rightarrow 0 \text{ sec}$

The two substrates as thus produced were paired in such a manner that the porous layers were directed outwardly, that is, back to back, and five pairs were set by a holder made of quartz glass so that five pairs were kept at intervals of 1 cm. This was set in a load

lock chamber of the apparatus shown in Fig. 4, and after the door was closed, atmosphere inside thereof was replaced by nitrogen.

Then, the gate valve 405 was opened, and the substrate 416 supported by the substrate holder was transported to the vapor phase growth vessel 404. After transportation, the gate valve 405 was closed, the inside was replaced by hydrogen, and the temperature of the substrate started to elevate while hydrogen was allowed to flow into the vessel. When the temperature was elevated up to 1,000°C, that state was kept for 30 minutes, during which the smoothing of the porous layer surface was progressed.

Then, the first n⁺ type crystal silicon layer of 0.2 μm in thickness was deposited under the condition shown in Table 10. Upon the completion of growth, while the inside of the vapor phase growth vessel 404 was replaced by hydrogen, the temperature of the substrate holder was lowered to 900°C.

Table 10

Gas Flow Amount /min	SiH ₂ Cl ₂ /PH ₃ /H = 0.5 l/0.2 cc/100 l
Substrate Temperature	1,000°C
Pressure	Atmospheric pressure
Growth time	1 min

On the other hand, after the completion of growth, the inside of the vapor phase growth vessel 404 was

replaced by hydrogen. In a liquid phase growth vessel 409, silicon was dissolved at 900°C into a metal indium solvent within a boat 414 up to a concentration with which the solvent was just saturated, and stirred so that the solution was uniform. Upon the completion of adjustment of melting, a gate valve 410 was opened, and a substrate holder 416 was immersed into the melted material 415. Then cooling was gradually conducted at a cooling rate of -1°C/min. After 25 minutes, the gate valve 410 was opened and the substrate holder 416 was lifted up. Active layer having a thickness of 20 μm was deposited. The substrate holder 416 was received in the vapor phase growth vessel 404, and the gate valve 410 was closed. Here, the third P⁺ type crystal silicone layer of 0.5 μm in thickness was deposited again by the vapor phase growth method under the condition shown in Table 11 (Fig. 5C).

Table 11

Gas Flow Amount /min	$\text{SiH}_2\text{Cl}_2/\text{B}_2\text{H}_6/\text{H}_2 = 1 \text{ l}/0.5 \text{ cc}/100 \text{ l}$
Substrate Temperature	1,000°C
Pressure	Atmospheric pressure
Growth time	2 min

Upon the completion of growth, hydrogen was allowed to flow to wait the cool down of the substrate holder 416. When the temperature of the substrate holder 416 was lowered to 200°C, the gate valve 405 was

opened to transport the substrate holder 416 to the load lock chamber 401. After the door was closed, atmosphere inside thereof was replaced by nitrogen, and then the substrate holder 416 was taken out of the apparatus.

The copper paste was coated in thickness of 20 μm on one surface of the polyimide film having a thickness of 50 μm which was the second substrate by screen printing, and that surface was brought in close contact with and bonded to the surface of the above-mentioned wafer p⁺ type thin-film silicon layer. In this state, it was conveyed into an oven so that the copper paste was sintered under the condition of 300°C and 20 minutes, and the polyimide film and the wafer were bonded onto each other (Fig. 5D).

In the polyimide film and the wafer as bonded onto each other, another surface of the wafer which was not bonded was fixed by a vacuum chuck (not shown in the drawing), and a force was exerted from one end of the polyimide film to conduct peeling in such a manner that the n⁺ type silicon layer, the active silicon layer and the p⁺ type silicon layer were separated from the wafer and then transferred onto the polyimide film (Fig. 5E).

The remainder of the porous layer which remained on the thin-film silicon layer separated from the wafer was selectively etched while being stirred with a

mixture solution consisting of hydrofluoric acid, hydrogen peroxide and pure water. The thin-film silicon layer remained without being etched, and only the remainder of the porous layer is completely removed (Fig. 5F). In the non-porous silicon single-crystal, the etching rate by using the above-mentioned etching solution is very low, and the selective ratio by the etching rate of porous silicon layer to that of non-porous silicon layer reaches 10^5 or more so that the etching amount of the porous layer (about several tens Å) can be ignored in practical use. As a result of observing the section of the layer by a transparent electron microscope, it has been recognized that excellent crystallinity is maintained such that a new crystal defect is not introduced in the thin-film silicon layer.

Finally, an ITO transparent conductive film (82 nm thick) and a collecting electrode (Ti/Pd/Ag (400 nm/200 nm/1 μ m thick)) are formed on the n^+ type silicone layer by the EB (electron beam) vapor deposition to provide a solar cell (Fig. 5G).

As a result of measuring the I-V characteristic of the obtained polyimide thin-film/single-crystal silicon using solar cell thus under illumination of AM 1.5 (100 mW/cm^2) light, the conversion efficiency of 14.9% was obtained.

Also, the porous layer that remained on the

silicon wafer as separated was removed by etching in the same manner as described above to produce a smooth surface (Fig. 5H). By using the regenerated wafer thus obtained, the above-mentioned steps were repeated to obtain a plurality of thin-film single-crystal solar cells having a semiconductor layer with high quality.

(Example 14)

A solar cell was formed by the steps shown in Figs. 12A to 12M, using an apparatus shown in Fig. 4.

First, a p^+ type region 1201 was formed in the surface of, as a substrate, B was thermally diffused onto the surface of the single-crystal silicon wafer having a thickness of 500 μm by using BCl_3 as the thermal diffusion source at a temperature of 1,200°C to form a P^+ type layer, thus obtaining a diffusion layer of about 3 μm in depth.

Then, anodization was conducted under the same condition as in Example 13 in an HF solution to form a porous silicon layer 202 on the wafer (Fig. 12B).

Subsequently, the p^+ type thin-film crystal silicon layer 206 was allowed to epitaxially grow under the same condition as in Example 13 by the vapor phase growth method (Fig. 12C).

Subsequently, similarly to Example 13, keeping the reducing atmosphere, the active layer 203 of a p^- type thin-film crystal silicon was allowed to epitaxially grow by the liquid phase growth method (Fig. 12D).

Again, the n⁺ type thin-film crystal silicon layer 204 was allowed to epitaxially grow under the same condition as in Example 13 by the vapor phase growth method (Fig. 12E).

5 At this stage, the wafer was taken out of the apparatus shown in Fig. 4, an ITO transparent electrode 706 was deposited through the commercially available sputtering apparatus (Fig. 12F).

10 Keeping the state, a water-soluble adhesive 707 for book binding (AGX-5137 manufactured by Nitta Gelatine Co.) was coated on the surface, and a water permeable substrate such as a commercially available cardboard 708 (the second substrate) was bonded thereonto and dried (Fig. 12G).

15 In this state, the silicon wafer 201 was vacuum chucked and a force was exerted on the cardboard 708. As a result, the porous layer 202 was destroyed and the semiconductor layer together with the cardboard 708 was peeled off from the wafer 201 (Fig. 12H).

20 The sample peeled off was then bonded onto a stainless steel plate 710 (the third substrate) coated with a copper paste 709, and was provisionally sintered at 150°C (Fig. 12I). Thereafter, hot water at 80°C was made to permeate from the back of the cardboard 708 to
25 thereby dissolve the adhesive 707 and peel off the semiconductor layer from the cardboard 708 (Fig. 12J).

 Thereafter, remainder of the adhesive 707 which

remained on the surface of the transparent electrode 706 was washed, and further a collecting electrode 711 was printed on the surface of the semiconductor layer with a copper paste. After conducting a provisional
5 sintering, it was fully sintered at 500°C (Fig. 12K). Copper has a high reflectance with respect to sun light which penetrates the semiconductor layer without being absorbed, thereby being capable of absorbing the light again by the semiconductor layer. Accordingly, even in
10 the solar cell using a relatively thin semiconductor layer, high efficiency can be obtained.

Further, in the step as shown in Fig. 12H, the porous layer 202 which remained after peeling off is not necessarily removed, because it does not cause a
15 functional obstacle which is a feature of this structure.

On the other hand, the remainder of the porous layer 702 that remained on the wafer 201 as separated in the step shown in Fig. 12H was removed by etching to
20 produce a smooth surface (Fig. 12L). Thereafter, the p⁺ type layer 1201' of about 3 μm in thickness was again formed by the liquid phase growth method (Fig. 13M). The above steps were repeated again using the silicone wafer 201, the solar cell was fabricated.

25 As a result of measuring the I-V characteristic of the obtained thin-film single-crystal silicon solar cell using the stainless plate under illumination of AM

1.5 (100 mW/cm²) light, the energy conversion efficiency of 15% or more was obtained with respect to the solar cells obtained by either the first or second cycle.

Further, according to the present invention, not only the method in which adhesive force is lowered by permeating water, but also another means of, for example, containing solvents, or any means that can lower the adhesive force may be applied to obtain the same functional effect.

(Example 15)

A solar cell was formed in the same manner as in Example 14 by the steps shown in Figs. 12A to 12M except that the doping was not carried out on the semiconductor layer 206 grown on the porous layer 202 in vapor phase. Further, when the active layer 203 was grown, the growth of silicone was terminated. In the vapor phase growth vessel 404 shown in Fig. 4, the surface of the silicon layer was heat treated at 1,200°C for one hour by the vapor phase diffusion method using POC₃ to thermally diffuse P in the vicinity of the surface of silicon. As a result, n⁺ type layer 204 was formed. At the same time, B in the P⁺ type porous layer was thermally diffused. As a result, the semiconductor layer 206 became P⁺ type.

Thereafter, the solar cell was formed in the same procedure as in Example 14 after the formation of the transparent electrode 706 (Fig. 12F). Further, the

wafer used was subjected to the same treatment and was reused, thereby being capable of fabricating the solar cell, newly.

As a result of measuring the I-V characteristic of the obtained thin-film single-crystal silicon solar cell on the stainless plate under illumination of AM 1.5 (100 mW/cm²) light, the energy conversion efficiency of 15% or more was obtained with respect to the solar cells obtained by either the first or second cycle.

(Example 16)

In this example, a stagger type field effect transistor is fabricated in the same manner as in Example 13.

In the same manner as in Example 13, B was thermally diffused into the surface of single-crystal silicon wafer 601 having a thickness of 500 μ m by using BCl₃ as a heat diffusion source at a temperature of 1,200°C to form a p⁺ type layer and obtain a diffusion layer of about 3 μ m in thickness. Then, a porous layer 802 was formed in the same manner in Example 1 (Figs. 10A and 10B).

Subsequently, sample was set on the apparatus shown in Fig. 4. Firstly, in the vapor phase vessel 404, an n⁺ type thin-film silicon layer 603 having a thickness of 0.1 μ m was deposited on the porous layer 602 (Fig. 10C).

Then, keeping the reducing atmosphere, the sample

was transported into the liquid phase growth vessel to deposit a P⁻ type thin-film silicon layer 604 was deposited, and then lifted up from the apparatus shown in Fig. 4 (Fig. 10D).

5 Subsequently, the surface side of the p⁻ type thin-film silicon layer 604 was oxidized to 0.1 μm in depth by the heat treatment in a steam to provide a gate insulated film 605 (Fig. 10E).

10 On the film, an aluminum film was deposited by the sputtering method, and a gate electrode/gate wiring 606 was formed by the photolithography process (Fig. 10F). On the film, the glass substrate 608 was stuck through the SiO₂ film 607 by the sol/gel method (Fig. 10G).

15 Thereafter, the wafer 601 was peeled off, and after the remainder of the porous layer 602 was removed (Fig. 10I), the n⁺ type thin-film silicon layer 603 was patterned as indicated by reference numeral 603' and 603" by the photolithography process. Moreover on the film, a silicon nitride layer was deposited, and
20 patterned by the photolithography process as indicated by reference numeral 609. Furthermore, an aluminum layer was deposited and patterned by the photolithography process, to thereby form the drain electrode/drain wiring 610' and the source
25 electrode/source wiring 610" (Figs. 10H to 10L).

 Since the transistor thus fabricated had p⁻ type layer of single-crystal and was thinned, it obtained

very high on/off ratio of the drain current than the on/off ratio of the gate voltage, and also obtained large on current. Therefore, even if the area of the transistor is small, a large driving performance is provided. Also, since it is of the stagger type using single-crystal, the degree of free of the drain/gate wiring is as large as that of the transistor using amorphous silicon, and when the transistor is used for the matrix driving of liquid crystal or the like, the high contrast, the high-speed operation and the high opening degree can be readily realized.

As was described above, according to the present invention, the semiconductor layer made of single-crystal which is excellent in crystallinity, polycrystal or the like, can be produced on the second substrate at the low costs. Also, the semiconductor member which can be variously used can be obtained by forming the semiconductor layer on the inexpensive and flexible substrate.

Also, according to the present invention, the thin-film crystal solar cell with high conversion efficiency can be obtained on the low-heat-resistant substrate, thereby being capable of providing the solar cells with excellent mass production and high quality to the market.

Also, according to the present invention, there can be provided a method of producing a semiconductor

member in which crystal semiconductor excellent in various characteristics can be formed even on a substrate which is not high-temperature resistant and a method of producing a solar cell using the semiconductor member.

Further, according to the present invention, there can be provided a method of producing a semiconductor member in which crystal semiconductor excellent in various characteristics can be formed even on a flexible substrate and a method of producing a solar cell using the semiconductor member.

Further, according to the present invention, there can be provided a method of producing a semiconductor member which can be variously applied, used and arranged and a method of producing a solar cell using the semiconductor member.

Further, according to the present invention, there can be provided a method of producing a semiconductor member having excellent semiconductor characteristics at low costs and a method of producing at low costs a solar cell and exhibiting various characteristics such as excellent photoelectric conversion characteristics or use characteristics by using the semiconductor member.

Further, according to the present invention, there can be provided a method of producing a solar cell which can exhibit high conversion efficiency.

Further, according to the present invention, there can be provided a semiconductor member which can be obtained by peeling off an epitaxial layer formed on a crystal substrate from the crystal substrate and the
5 crystal substrate to be reused, and a semiconductor member with more high performance which is produced at low costs by use of an inexpensive raw material.

Further, according to the present invention, there can be provided a solar cell which is formed by using a
10 semiconductor member and the crystal substrate to be reused, and a semiconductor member with more high performance and which is produced at low costs by use of an inexpensive raw material.

Also, as was described above, according to the
15 present invention, the thin semiconductor layer is allowed to grow on the single-crystal substrate by the vapor phase growth method in which the crystal growth is readily controlled, and the conveying conditions are strictly controlled. Sequentially, the crystal
20 semiconductor layer having the least thickness necessary for absorbing a solar light can be allowed to epitaxially grow by the liquid phase method which is reduced in the raw material costs before being separated, and the expensive substrate can be repeated
25 used, thereby being capable of providing a flexible solar cell with high efficiency at low costs.

Further, since the reducing atmosphere is always

maintained, the thin-film semiconductor layer having a high-quality joint can be readily obtained.

Further, the polycrystal substrate or the substrate with high impurity concentration can be also
5 used as the substrate, thereby being capable of more reducing the costs.

Further, the thin-film crystal solar cell with high conversion efficiency can be obtained on the low-heat-resistant substrate, thereby being capable of
10 providing the solar cells with excellent mass production and high quality to the market. Further, in order to compensate a reduction of the thickness of the first substrate which is accompanied by the formation and separation of the porous layer, the
15 crystal layer is allowed to grow on the surface of the first substrate by the liquid phase growth method, thereby being capable of effectively utilizing the first substrate and also optimizing the porous layer without being directly affected by the quality of the
20 substrate.

Further, there can be obtained the transistor which is excellent in characteristics so as to provide a large driving performance even though the area of the transistor is small, in the case of preparing the
25 transistor by using the method of producing the semiconductor member according to the present invention. Also, since the stagger type field effect

transistor using the above-mentioned single-crystal as described in the above Examples can be readily fabricated, the degree of freedom of the drain/gate wiring is increased as much as the transistor using amorphous silicon. In the case of using the transistor for liquid-crystal matrix drive, etc., high contrast, high-speed operation and high opening ratio can be readily realized.

In addition, by using the semiconductor member obtained according to the method of the present invention, semiconductor devices such as an LED (Light Emitting Device) other than the transistor and the solar cell can be formed on a flexible substrate or an insulating substrate. The semiconductor member of the present invention is a so-called SOI (semiconductor on insulator) having the semiconductor layer excellent in various characteristics, and is very useful.

WHAT IS CLAIMED IS:

1. A method of producing a semiconductor member,
comprising the steps of:

5 forming a porous layer in a surface region of a
first substrate;

forming a semiconductor layer on the porous layer
by liquid phase epitaxy;

10 bonding a second substrate to a surface of the
semiconductor layer opposite to a semiconductor layer
surface bonded to the first substrate; and

separating the first substrate from the
semiconductor layer by utilizing the porous layer to
transfer the semiconductor layer to the second
substrate.

15

2. A method according to claim 1, wherein the
semiconductor layer is formed on the porous layer, the
semiconductor layer comprising a region formed by vapor
phase epitaxy and a region formed by the liquid phase
20 epitaxy in this order.

20

3. A method according to claim 1, further
comprising a step of removing the porous layer
remaining on the surface of the first substrate after
25 the first substrate is separated from the semiconductor
layer.

25

4. A method according to claim 1, wherein the liquid phase epitaxy is conducted using a melting solution in which elements for forming the semiconductor layer to be grown are dissolved up to a supersaturated state or a substantially supersaturated state.

5. A method according to claim 1, wherein the liquid phase epitaxy is conducted under a reducing atmosphere.

6. A method according to claim 1, wherein the liquid phase epitaxy includes that a melting solution in which elements for forming the semiconductor layer to be grown are dissolved is brought in contact with the porous layer.

7. A method according to claim 1, wherein the liquid phase epitaxy includes that a melting solution in which elements for forming the semiconductor layer to be grown are dissolved is brought in contact with an epitaxial layer formed on the porous layer.

8. A method according to claim 7, wherein the epitaxial layer is formed by vapor phase epitaxy.

9. A method according to claim 1, wherein the

liquid phase epitaxy includes that a melting solution in which elements for forming the semiconductor layer to be grown are dissolved upto a desired concentration is used and the melting solution is brought in contact with a surface of the porous layer while a surface temperature of the porous layer is made lower than a temperature at which the elements in the melting solution having the desired concentration are saturated.

10. A method according to claim 2, wherein the vapor phase epitaxy is conducted by decomposing a source gas while supplying a gas for forming a reducing atmosphere.

11. A method according to claim 1, wherein the step of bonding the second substrate is conducted using an adhesive.

12. A method according to claim 11, wherein the adhesive comprises a water-soluble adhesive.

13. A method according to claim 1, further comprising a step of providing a third substrate on a separate surface for transferring the semiconductor layer to the second substrate.

14. A method according to claim 13, further comprising a step of separating the second substrate to transfer the semiconductor layer onto the third substrate.

5

15. A method according to claim 1, wherein the second substrate has a water permeability.

10 16. A method according to claim 14, wherein the separation of the second substrate is conducted by the deterioration of adhesion of the adhesive used for bonding of the second substrate.

15 17. A method according to claim 16, wherein the deterioration of the adhesion is conducted by a liquid that has passed through the second substrate.

20 18. A method according to claim 16, wherein the adhesive is water-soluble, and the deterioration of the adhesion is conducted by a water that permeates the second substrate.

25 19. A method according to claim 1, wherein an impurity in the porous layer is diffused into the semiconductor layer.

20. A method according to claim 1, wherein the

liquid phase epitaxy is conducted with indium as a solvent.

21. A method of producing a solar cell,
5 comprising the steps of:
forming a porous layer in a surface region of a first substrate;
forming a semiconductor layer on the porous layer by liquid phase epitaxy;
10 bonding a second substrate to a surface of the semiconductor layer opposite to a semiconductor layer surface bonded the first substrate; and
separating the first substrate from the semiconductor layer by utilizing the porous layer to
15 transfer the semiconductor layer to the second substrate.

22. A method according to claim 21, wherein the semiconductor layer is formed on the porous layer, the
20 semiconductor layer comprising a region formed by vapor phase epitaxy and a region formed by liquid phase epitaxy in this order.

23. A method according to claim 21, further
25 comprising a step of removing the porous layer remaining on the surface of the first substrate after the first substrate is separated from the semiconductor

layer.

24. A method according to claim 21, wherein the liquid phase epitaxy is conducted using a melting
5 solution in which elements for forming the semiconductor layer to be grown are dissolved up to a supersaturated state or a substantially supersaturated state.

10 25. A method according to claim 21, wherein the liquid phase epitaxy is conducted under a reducing atmosphere.

15 26. A method according to claim 21, wherein the liquid phase epitaxy includes that a melting solution in which elements for forming the semiconductor layer to be grown are dissolved is brought in contact with the porous layer.

20 27. A method according to claim 21, wherein the liquid phase epitaxy includes that a melting solution in which elements for forming the semiconductor layer to be grown are dissolved is brought in contact with an epitaxial layer formed on the porous layer.

25

28. A method according to claim 27, wherein the epitaxial layer is formed by vapor phase epitaxy.

29. A method according to claim 21, wherein the liquid phase epitaxy includes that a melting solution in which elements for forming the semiconductor layer to be grown are dissolved upto a desired concentration is used and the melting solution is brought in contact with a surface of the porous layer while a surface temperature of the porous layer is made lower than a temperature at which the elements in the melting solution having the desired concentration are saturated.

30. A method according to claim 22, wherein the vapor phase epitaxy is conducted by decomposing a source gas while supplying a gas for forming a reducing atmosphere.

31. A method according to claim 21, wherein the bonding step of the second substrate is conducted using an adhesive.

32. A method according to claim 31, wherein the adhesive includes a water-soluble adhesive.

33. A method according to claim 21, further comprising a step of providing a third substrate on a separate surface for transferring the semiconductor layer onto the second substrate.

34. A method according to claim 33, further comprising a step of separating the second substrate to transfer the semiconductor layer onto the third substrate.

5

35. A method according to claim 21, wherein the second substrate has a water permeability.

36. A method according to claim 34, wherein the separation of the second substrate is conducted by the deterioration of adhesion of the adhesive used for bonding of the second substrate.

37. A method according to claim 36, wherein the deterioration of the adhesion is conducted by a liquid that has passed through the second substrate.

38. A method according to claim 36, wherein the adhesive is water-soluble, and the deterioration of the adhesion is conducted by a water that permeates the second substrate.

39. A method according to claim 21, wherein an impurity in the porous layer is diffused into the semiconductor layer.

40. A method according to claim 21, wherein the

liquid phase epitaxy is conducted with indium as a solvent.

41. A method according to claim 21 wherein before
5 the bonding of the second substrate, an impurity is
introduced into the semiconductor layer.

42. A method according to claim 21 wherein before
the bonding of the second substrate, an impurity is
10 introduced into the semiconductor layer to form a p-n
junction.

43. A method according to claim 21 wherein the
second substrate has an electroconductive surface.
15

44. A method according to claim 21, further
comprising a step of removing the porous layer
remaining on the transferred semiconductor layer.

45. A method according to claim 21, further
20 comprising a step of forming an electrode on the
transferred semiconductor layer.

46. A method according to claim 21, further
25 comprising a step of introducing an impurity into the
transferred semiconductor layer.

47. A method according to claim 21, further comprising a step of forming a semiconductor layer containing an impurity on the transferred semiconductor layer.

5

48. A method according to claim 3, further comprising a step of forming a semiconductor layer by conducting epitaxial growth on the substrate from which the porous layer is removed.

10

49. A method according to claim 48, wherein the semiconductor layer formed by conducting epitaxial growth has p-type or n-type conductivity.

15

50. A method according to claim 23, further comprising a step of forming a semiconductor layer by conducting epitaxial growth on the substrate from which the porous layer is removed.

20

51. A method according to claim 50, wherein the semiconductor layer formed by conducting epitaxial growth has p-type or n-type conductivity.

25

52. A method of producing a semiconductor member, the method comprising the steps of:

(a) forming a porous layer in a surface region of a first substrate;

(b) immersing the porous layer into a melting solution in which elements for forming a semiconductor layer to be grown is dissolved up to a supersaturated state or a substantially supersaturated state under a reducing atmosphere to grow a semiconductor layer on a surface of the porous layer;

(c) bonding a second substrate onto a surface side of the first substrate on which at least the porous layer and the semiconductor layer are formed; and

(d) separating the first substrate from the second substrate at the porous layer to transfer the semiconductor layer separated from the first substrate to the second substrate.

53. A method of producing a semiconductor member according to claim 52, wherein a surface of the first substrate separated in the step (d) is treated and then again subjected to the step (a) as the first substrate.

54. A method of producing a semiconductor member claimed according to claim 52, wherein after a surface of the first substrate separated in the step (d) is treated, a semiconductor layer into which an impurity is introduced by liquid phase growth is allowed to grow on the surface of the first substrate, and then again subjected to the step (a) as the first substrate.

55. A method of producing a semiconductor member according to claim 54, wherein prior to the formation of the semiconductor layer in which the impurity is introduced, a semiconductor layer into which no
5 impurity is introduced or impurity is introduced with a small concentration is formed on the surface of the first substrate after being subjected to the surface treatment.

10 56. A method of producing a semiconductor member according to claim 54, wherein semiconductor having a purity of 99.99% or less is used as the first substrate.

15 57. A method of producing a semiconductor member, the method comprising the steps of:

(a) forming a porous layer in a surface region of a first substrate;

(b) immersing, into a melting solution in which
20 elements for forming a semiconductor layer to be grown is dissolved up to a desired concentration, the porous layer whose surface temperature is made lower than a temperature at which the melting solution having the desired concentration is saturated, to grow a
25 semiconductor layer on a surface of the porous layer;

(c) bonding a second substrate onto a surface side of the first substrate on which at least the porous

layer and the semiconductor layer are formed; and

(d) separating the first substrate from the second substrate at the porous layer to transfer the semiconductor layer separated from the first substrate to the second substrate.

58. A method of producing a semiconductor member according to claim 57, wherein a surface of the first substrate separated in the step (d) is treated and then again subjected to the step (a) as the first substrate.

59. A method of producing a semiconductor member according to claim 57, wherein after a surface of the first substrate separated in the step (d) is treated, a semiconductor layer into which an impurity is introduced by liquid phase growth is allowed to grow on the surface of the first substrate, and then again subjected to the step (a) as the first substrate.

60. A method of producing a semiconductor member according to claim 59, wherein prior to the formation of the semiconductor layer in which the impurity is introduced, a semiconductor layer into which no impurity is introduced or an impurity is introduced with a small concentration is formed on the surface of the first substrate after being subjected to the surface treatment.

61. A method of producing a semiconductor member according to claim 59, wherein semiconductor having a purity of 99.99% or less is used as the first substrate.

5

62. A method of producing a semiconductor member according to claim 52, wherein the first substrate is crystalline.

10

63. A method of producing a semiconductor member according to claim 52, wherein the first substrate is made of silicon single-crystal.

15

64. A method of producing a solar cell, comprising a step of using the semiconductor layer transferred to the second substrate which is obtained by the method of claim 52.

20

65. A method of producing a semiconductor member according to claim 57, wherein the first substrate is crystalline.

25

66. A method of producing a semiconductor member according to claim 57, wherein the first substrate is made of silicon single-crystal.

67. A method of producing a solar cell,

comprising a step of using the semiconductor layer transferred onto the second substrate which is obtained by the method of claim 57.

5 68. A method of producing a semiconductor member, the method comprising the steps of:

(a) forming a porous layer in a surface region of a first crystalline substrate;

10 (b) growing a first thin-film semiconductor layer on a surface of the porous layer in vapor phase by decomposing a source gas;

15 (c) immersing the first thin-film semiconductor layer into a melting solution in which elements for forming a second thin-film semiconductor are dissolved up to a saturated state or a supersaturated state under a reducing atmosphere to grow a second thin-film semiconductor layer of a conductive type different from that of the first thin-film semiconductor layer on a surface of the first thin-film semiconductor layer in liquid phase;

20 (d) bonding a second substrate onto a surface of the second thin-film semiconductor layer or onto a surface of a layer further formed on the second thin-film semiconductor layer;

25 (e) separating the first thin-film semiconductor layer from the first substrate by exerting a force on the porous layer to transfer the first thin-f

semiconductor layer to the second substrate.

69. A method of producing a semiconductor member according to claim 68, wherein the step of bonding the second substrate is conducted by using an adhesive.

70. A method of producing a semiconductor member according to claim 69, wherein the adhesive is a water-soluble adhesive.

71. A method of producing a semiconductor member according to claim 68, further comprising the steps of:
bonding a third substrate onto a separation surface of the substrate; and
separating the thin-film semiconductor layer from the second substrate to transfer the thin-film semiconductor layer to the third substrate.

72. A method of producing a semiconductor member according to claim 68, wherein the second substrate has a water permeability.

73. A method of producing a semiconductor member according to claim 71, wherein the step of separating the thin-film semiconductor layer bonded with an adhesive from the second substrate to transfer the thin-film semiconductor layer to the third substrate is

conducted by lowering adhesion of the adhesive.

74. A method of producing a semiconductor member according to claim 71, wherein the step of separating the thin-film semiconductor layer bonded with an adhesive from the second substrate to transfer the thin-film semiconductor layer to the third substrate is conducted by lowering adhesion of the adhesive through the second substrate.

75. A method of producing a semiconductor member according to claim 71, wherein the step of separating the thin-film semiconductor layer from the second substrate to transfer the thin-film semiconductor layer to the third substrate is conducted by adding a water to the second substrate having a water permeability to lower adhesion of the adhesive.

76. A method of producing a semiconductor member according to claim 71, wherein the step of separating the thin-film semiconductor layer bonded with a water-soluble adhesive from the second substrate to transfer the thin-film semiconductor layer to the third substrate is conducted by adding a water to the water-soluble adhesive to lower adhesion of the adhesive.

77. A method of producing a semiconductor member

according to claim 71, wherein the step of separating the thin-film semiconductor layer bonded with a water-soluble adhesive from the second substrate having a water permeability to transfer the thin-film semiconductor layer to the third substrate is conducted by adding a water to the water-soluble adhesive through the second substrate having a water permeability to lower adhesion of the adhesive.

10 78. A method of producing a semiconductor member according to claim 68, further comprising a step of treating a surface of the first substrate after being subjected to the operation and then reusing the treated first substrate.

15 79. A method of producing a semiconductor member according to claim 78, further comprising, after the surface of the first substrate from which the first thin-film semiconductor layer has been separated is
20 treated, a step of growing a semiconductor layer having the same composition as that of the first substrate and doped with an impurity on the surface of the first substrate in liquid phase, and then repeating the steps (a) to (e).

25 80. A method of producing a semiconductor member according to claim 79, further comprising, prior to the

formation of the semiconductor layer doped with the impurity, a step of forming a semiconductor layer doped with no impurity or doped with a small content of an impurity on the treated surface of the first substrate
5 by liquid phase growth, and then repeating the steps (a) to (e).

81. A method of producing a semiconductor member according to claim 68, wherein semiconductor having a
10 purity of 99.99% or less is used as the first substrate.

82. An apparatus of producing a semiconductor member in which a substrate comprising a porous layer
15 is stored and a semiconductor layer is formed on the porous layer, the apparatus comprising:

a liquid phase growth vessel for immersing a first thin-film semiconductor layer into a melting solution in which elements for forming a second thin-film
20 semiconductor layer are dissolved up to a saturated state or a supersaturated state under a reducing atmosphere to grow a second thin-film semiconductor layer on a surface of the first thin-film semiconductor layer in liquid phase; and

25 means for conveying the substrate between a vapor phase growth vessel and the liquid phase growth vessel while keeping the reducing atmosphere.

83. An apparatus according to claim 82, further comprising a vapor phase growth vessel disposed in front of the liquid phase growth vessel, for decomposing a source gas in the reducing atmosphere to
5 grow the first thin-film semiconductor layer on a porous layer surface of the substrate in vapor phase.

84. A method of producing a solar cell by using the method of claim 68 of producing the semiconductor
10 member.

85. An apparatus of producing a solar cell in which a substrate comprising a porous layer is stored and a semiconductor layer is formed on the porous
15 layer, the apparatus comprising:

a liquid phase growth vessel for immersing a first thin-film semiconductor layer into a melting solution in which elements for forming a second thin-film semiconductor layer are dissolved up to a saturated
20 state or a supersaturated state under a reducing atmosphere to grow a second thin-film semiconductor layer having a different conductivity type from that of the first thin-film semiconductor layer on a surface of the first thin-film semiconductor layer in liquid
25 phase; and

means for conveying the substrate between a vapor phase growth vessel and the liquid phase growth vessel

while keeping the reducing atmosphere.

86. An apparatus according to claim 85, further
comprising a vapor phase growth vessel disposed in
5 front of the liquid phase growth vessel, for
decomposing a source gas in the reducing atmosphere to
grow the first thin-film semiconductor layer on a
porous layer surface of the substrate in vapor phase.

ABSTRACT OF THE DISCLOSURE

To accomplish both of higher performance of a crystal and lower cost in a semiconductor member, and to produce a solar cell having a high efficiency and a flexible shape at low cost, the semiconductor member is produced by the following steps, (a) forming a porous layer in the surface region of a substrate, (b) immersing the porous layer into a melting solution in which elements for forming a semiconductor layer to be grown is dissolved, under a reducing atmosphere at a high temperature, to grow a crystal semiconductor layer on the surface of the porous layer, (c) bonding another substrate onto the surface of the substrate on which the porous layer and the semiconductor layer are formed and (d) separating the substrate from the another substrate at the porous layer.

FIG. 1

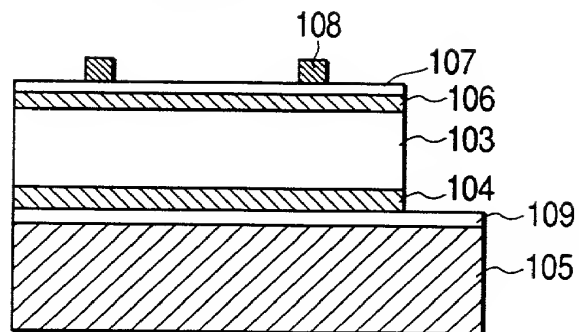


FIG. 3

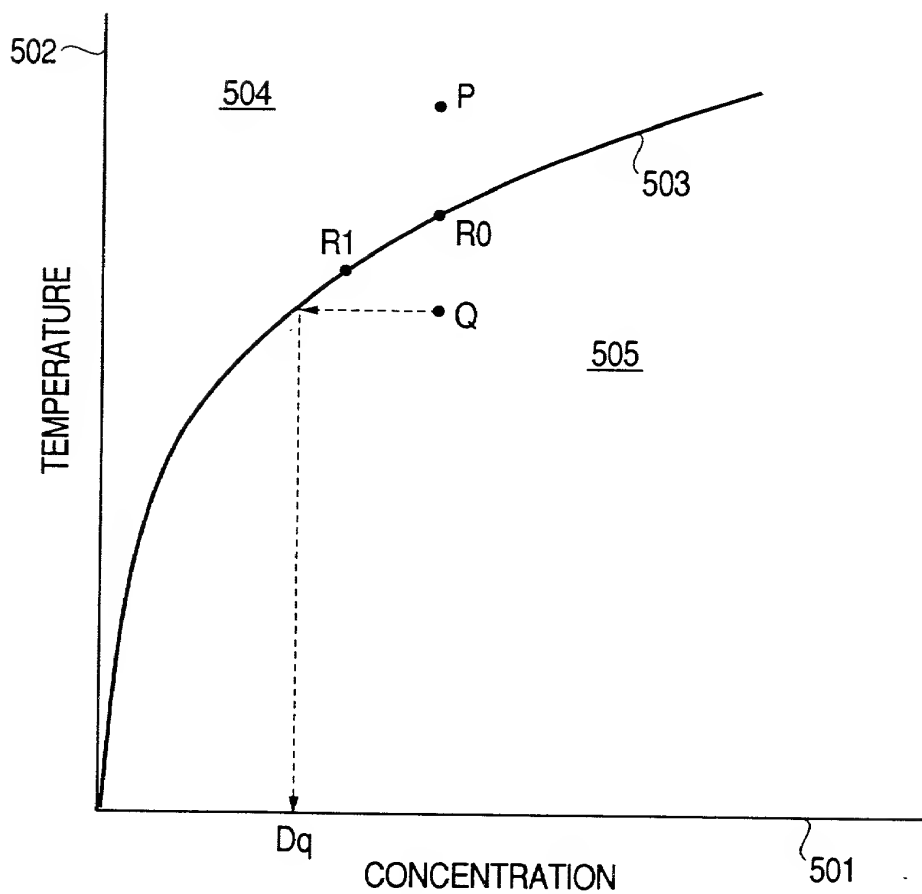


FIG. 2A

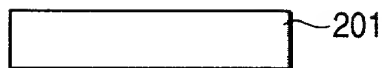


FIG. 2B

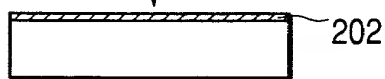


FIG. 2C

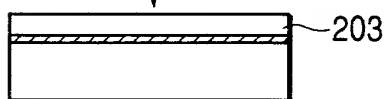


FIG. 2D

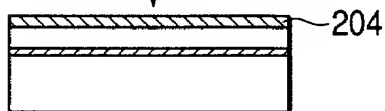


FIG. 2E

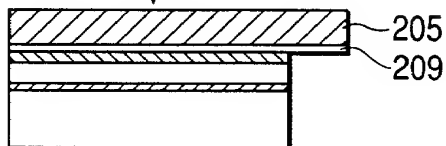


FIG. 2F

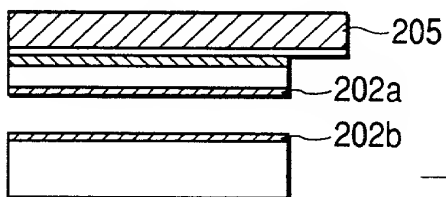


FIG. 2G

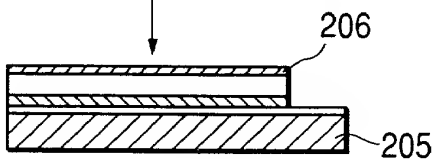


FIG. 2H

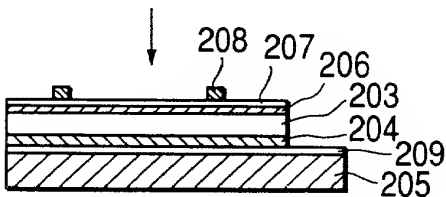


FIG. 2I



FIG. 4

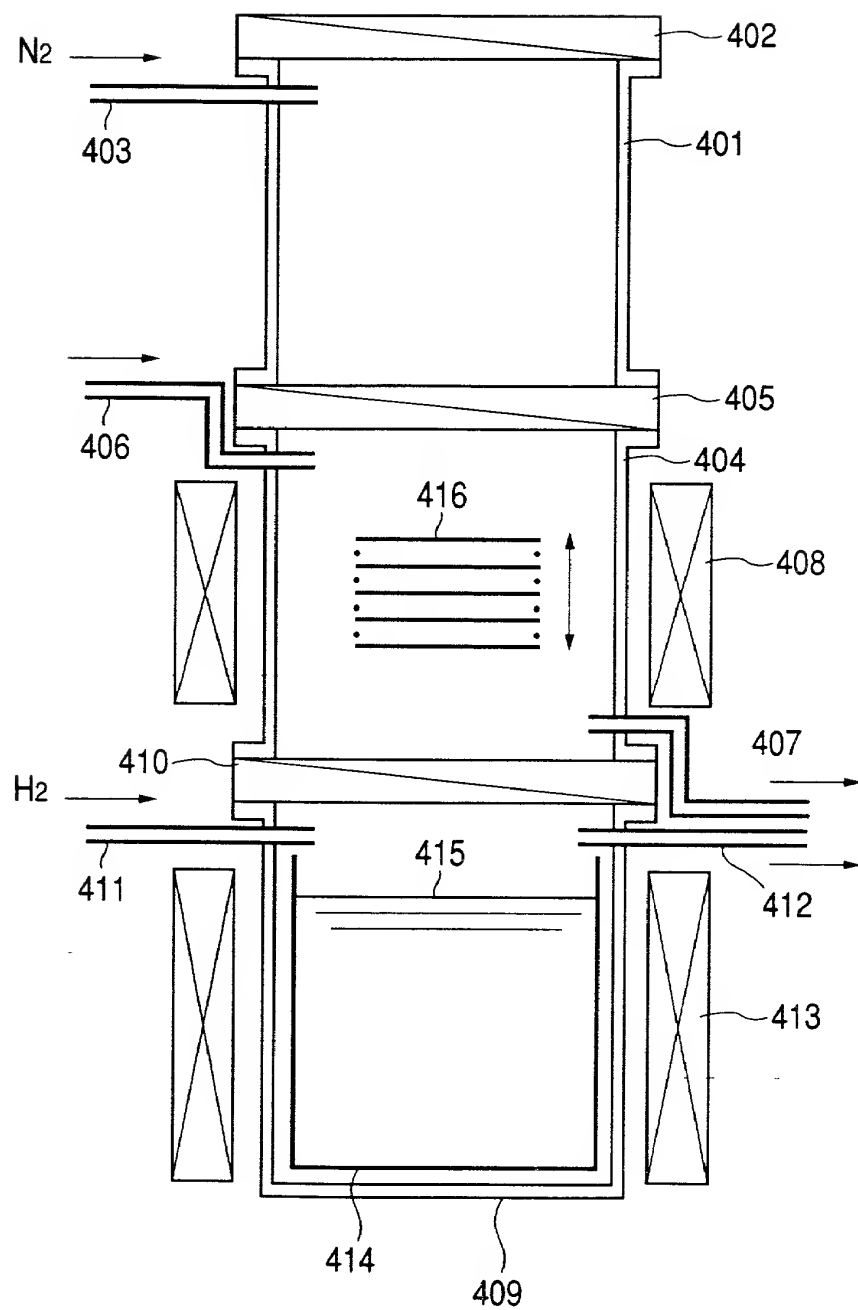


FIG. 5A



FIG. 5B

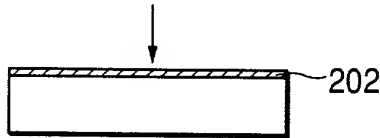


FIG. 5C

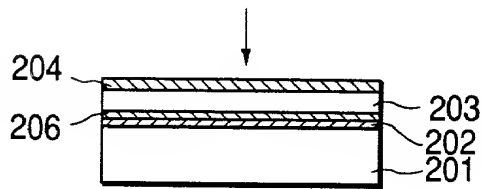


FIG. 5D

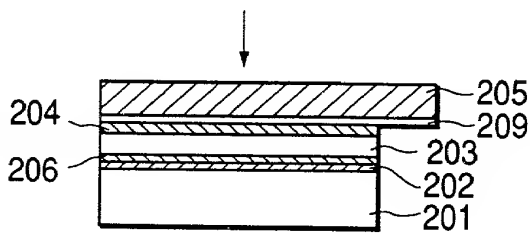


FIG. 5E

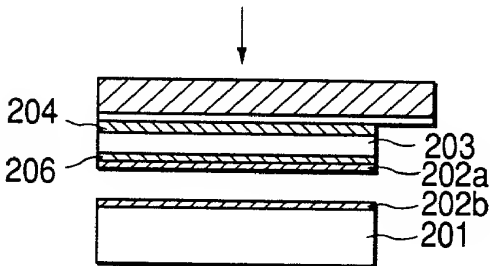


FIG. 5F

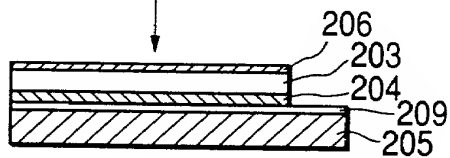


FIG. 5G

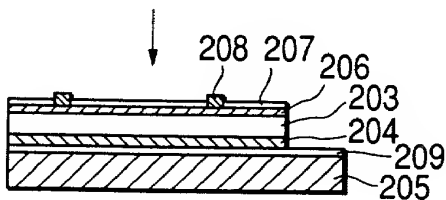


FIG. 5H

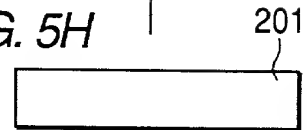


FIG. 6

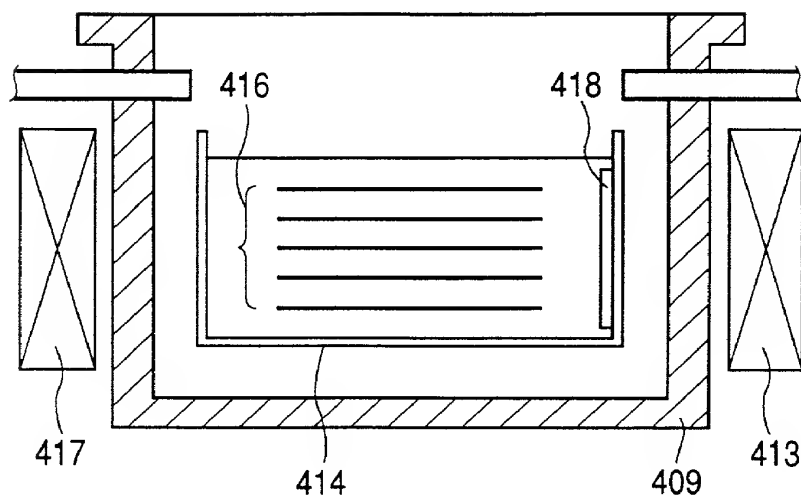


FIG. 7

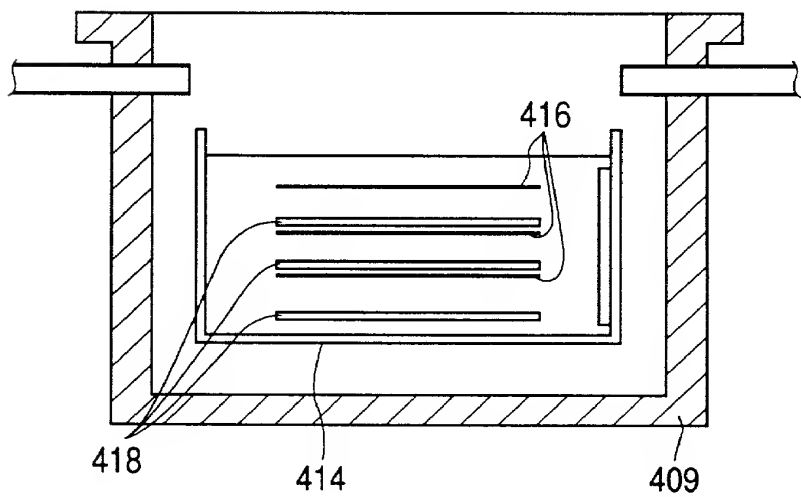


FIG. 8B



FIG. 8C

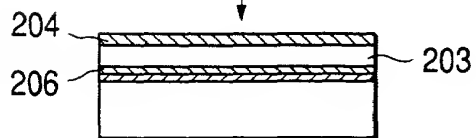


FIG. 8D

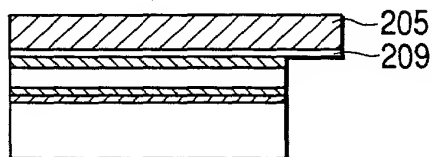


FIG. 8E

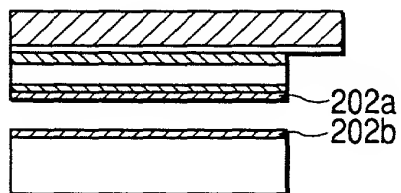


FIG. 8F

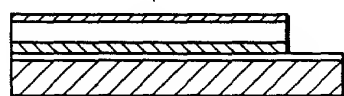


FIG. 8G

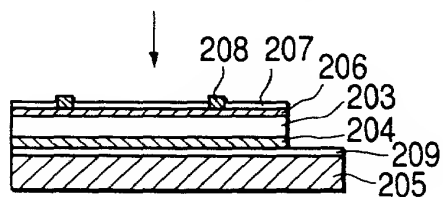


FIG. 8H

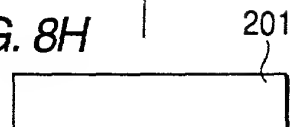


FIG. 9

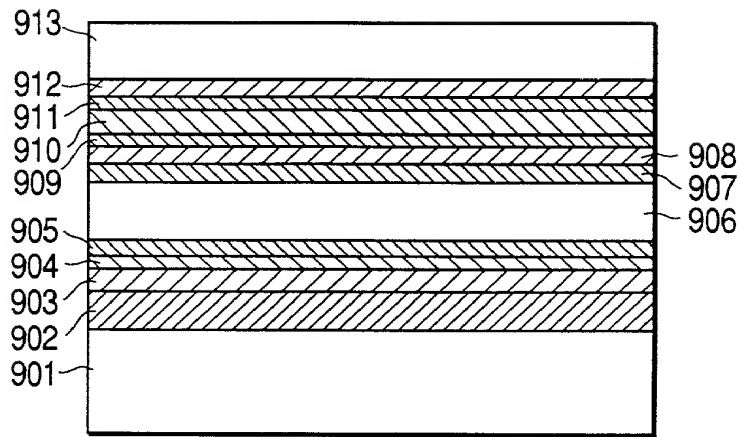


FIG. 10A



FIG. 10B

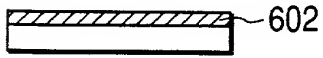


FIG. 10C

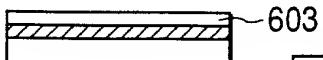


FIG. 10D

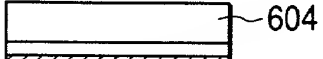


FIG. 10E

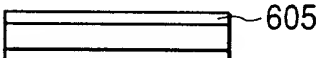


FIG. 10F

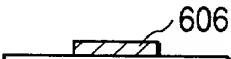


FIG. 10G

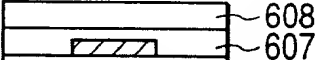


FIG. 10H

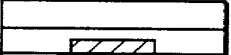


FIG. 10M



FIG. 10I

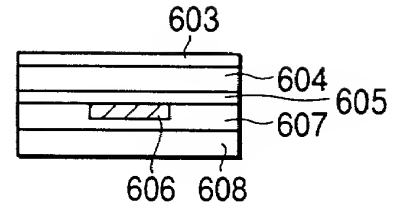


FIG. 10J

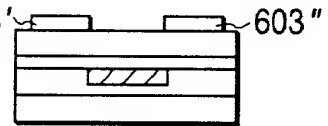


FIG. 10K

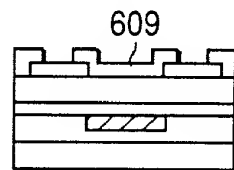


FIG. 10L

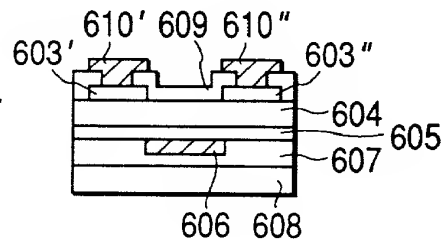


FIG. 11A



FIG. 11B

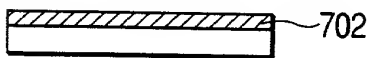


FIG. 11C

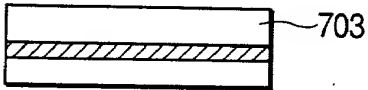


FIG. 11D

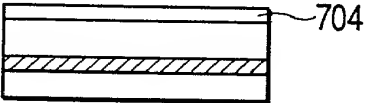


FIG. 11E

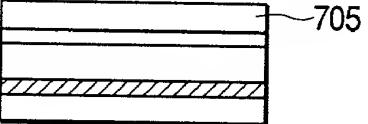


FIG. 11F

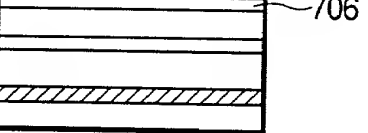


FIG. 11G

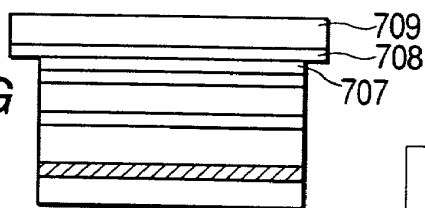


FIG. 11I

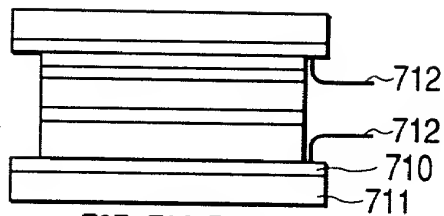


FIG. 11H

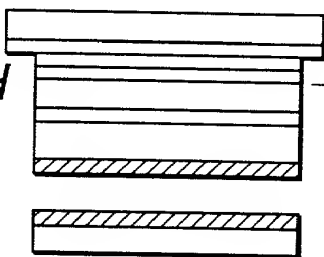
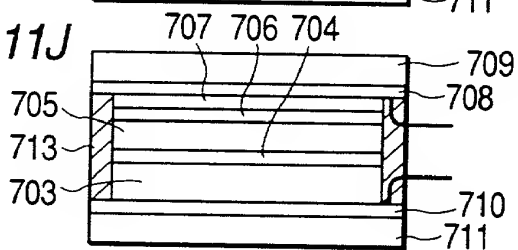
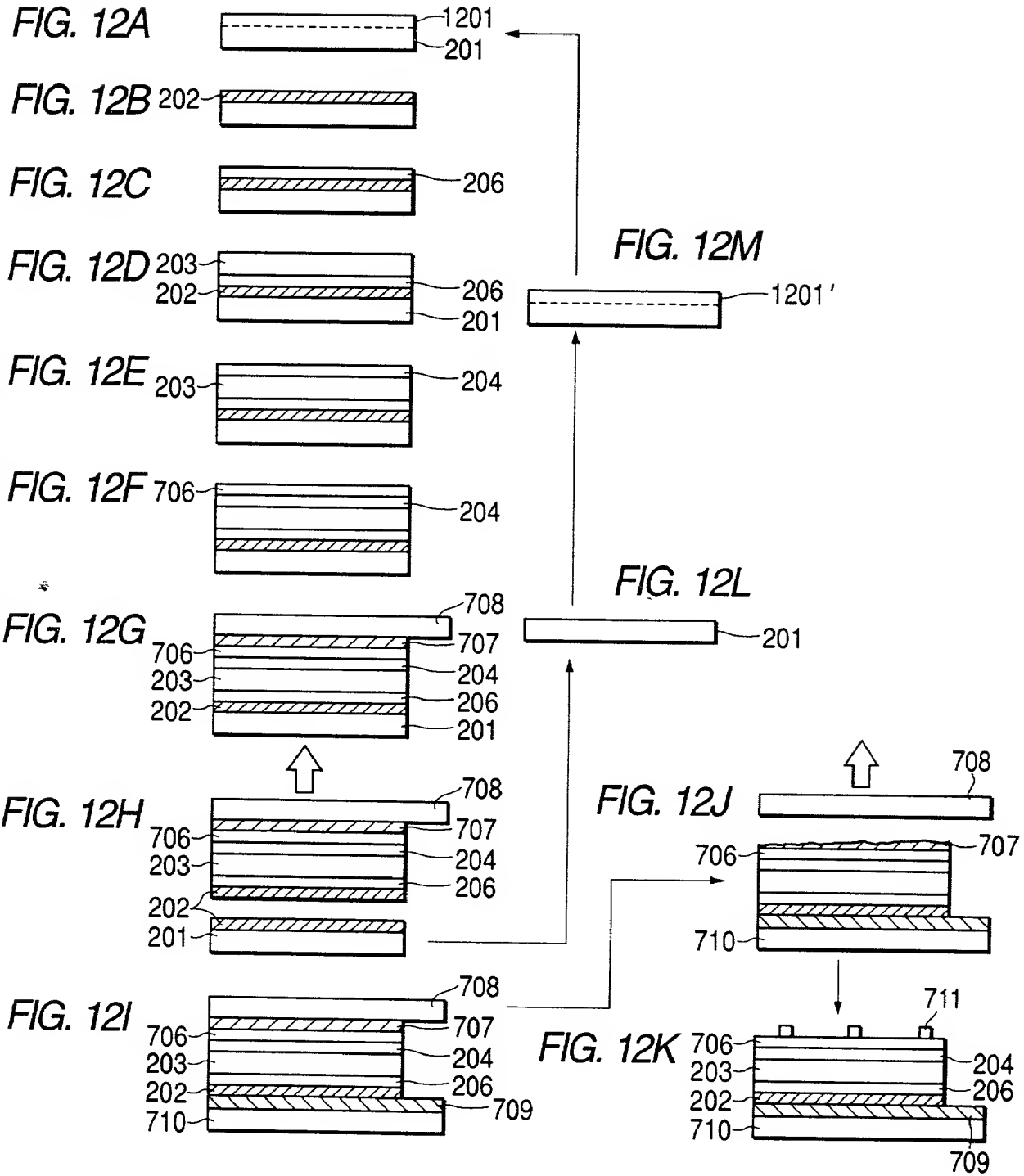


FIG. 11J





COMBINED DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION

COPY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled METHOD OF PRODUCING SEMICONDUCTOR MEMBER AND METHOD OF PRODUCING SOLAR CELL

_____, the specification of which
☐ is attached hereto. ☒ was filed on December 29, 1997 as Application
No. 08/999,132

and was amended _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Country	Application No.	Filed (Day/Mo./Yr.)	Priority Claimed (Yes/No)
JAPAN	8-350132	27 December 1996	YES
JAPAN	8-350133	27 December 1996	YES

I hereby appoint Joseph M. Fitzpatrick (Registration No. 17,398), Lawrence F. Scinto (Registration No. 18,973), William J. Brunet (Registration No. 20,452), Robert L. Baechtold (Registration No. 20,860), John A. O'Brien (Registration No. 24,367), John A. Krause (Registration No. 24,613), Henry J. Renk (Registration No. 25,499), Peter Saxon (Registration No. 24,947), Anthony M. Zupcic (Registration No. 27,276), Charles P. Baker (Registration No. 26,702), Stevan J. Bosses (Registration No. 22,291), Edward E. Vassallo (Registration No. 29,117), Ronald A. Clayton (Registration No. 26,718), Lawrence A. Stahl (Registration No. 30,110), Laura A. Bauer (Registration No. 29,767), Leonard P. Diana (Registration No. 29,296), David M. Quinlan (Registration No. 26,641), Nicholas N. Kallas (Registration No. 31,530), William M. Wannisky (Registration No. 28,373), Lawrence S. Perry (Registration No. 31,865), Robert H. Fischer (Registration No. 30,051), Christopher Philip Wrist (Registration No. 32,078), Gary M. Jacobs (Registration No. 28,861), Michael K. O'Neill (Registration No. 32,622), Bruce C. Haas (Registration No. 32,734), Scott K. Reed (Registration No. 32,433), Scott D. Malpede (Registration No. 32,533), Fredrick M. Zullo (Registration No. 32,452), Richard P. Bauer (Registration No. 31,588), Warren E. Olsen (Registration No. 27,290), Abigail F. Cousins (Registration No. 29,292), Steven E. Warner (Registration No. 33,326), Thomas J. O'Connell (Registration No. 33,202), Aaron C. Deditch (Registration No. 33,865), Penina Wollman (Registration No. 30,816), David L. Schaeffer (Registration No. 32,716), Jack S. Cubert (Registration No. 24,245), Mark A. Williamson (Registration No. 33,628), John T. Whelan (Registration No. 32,448), Jean K. Dudek (Registration No. 30,938), Raymond R. Mandra (Registration No. 34,382), Dominick A. Conde (Registration No. 33,856), Steven C. Bauman (Registration No. 33,832), Pasquale A. Razzano (Reg. No. 25,512), John W. Behringer (Registration No. 23,086), Robert C. Kline (Registration No. 17,739), Mark J. Itri (Registration No. 36,171), William C. Hwang (Registration No. 36,169), Karin L. Williams (Registration No. 36,721), Michael P. Sandomato (Registration No. 35,345), Jack M. Arnold (Registration No. 25,823), John D. Carlin (Registration No. 37,292), Daniel S. Glueck (Registration No. 37,838), Victor J. Geraci (Registration No. 38,157), Joseph W. Ragusa (Registration No. 38,586), Brian L. Klock (Registration No. 36,570), Anne M. Maher (Registration No. 38,231), William J. Zak, Jr. (Registration No. 38,668), Thomas D. Pease (Registration No. 35,317), Bruce M. Wexler (Registration No. 35,409), and Robert S. Mayer (Registration No. 38,544) my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith

Address all correspondence to:

FITZPATRICK, CELLA, HARPER & SCINTO
277 Park Avenue
New York, N.Y. 10172
Telephone No. (212) 758-2400

COMBINED DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION

(Page 2)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole or First Inventor KATSUMI NAKAGAWA
Inventor's signature Katsumi Nakagawa
Date February 26, 1998 Citizen/Subject of JAPAN
Residence 8-28-105, Hyakurakuen 1-chome, Nara-shi,
Nara-ken, Japan
Post Office Address c/o Canon Kabushiki Kaisha
30-2, Shimomaruko 3-chome, Ohta-ku, Tokyo, Japan

Full Name of Second Joint Inventor, if any TAKAO YONEHARA
Second Inventor's signature Takao Yonehara
Date February 25, 1998 Citizen/Subject of JAPAN
Residence 2235-2, Nurumizu, Atsugi-shi, Kanagawa-ken,
Japan
Post Office Address c/o Canon Kabushiki Kaisha
30-2, Shimomaruko 3-chome, Ohta-ku, Tokyo, Japan

Full Name of Third Joint Inventor, if any SHOJI NISHIDA
Third Inventor's signature Shoji Nishida
Date February 27, 1998 Citizen/Subject of JAPAN
Residence 92044, Kameino, Fujisawa-shi, Kanagawa-ken,
Japan
Post Office Address c/o Canon Kabushiki Kaisha
30-2, Shimomaruko 3-chome, Ohta-ku, Tokyo, Japan

Full Name of Fourth Joint Inventor, if any KIYOFUMI SAKAGUCHI
Fourth Inventor's signature Kiyofumi Sakaguchi
Date March 2, 1998 Citizen/Subject of JAPAN
Residence 19-2-504, Eda Higashi 2-chome, Tsuzuki-ku,
Yokohama-shi, Kanagawa-ken, Japan
Post Office Address c/o Canon Kabushiki Kaisha
30-2, Shimomaruko 3-chome, Ohta-ku, Tokyo, Japan

Full Name of Fifth Joint Inventor, if any _____
Fifth Inventor's signature _____
Date _____ Citizen/Subject of _____
Residence _____
Post Office Address _____